GC9B71

a-Si TFT LCD Single Chip Driver

360RGBx360 Resolution

Rev.1.0

2020-10-15

GENERATION REVISION HISTORY

REV.	EFFECTIVE DATE	DESCRIPTION OF CHANGES	PREPARED BY
1.0	2020-10-15	New Created	Kelly

Table of Content

Introduction

GC9B71 is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 360RGBx360 dots, comprising a 540-channel source driver, a 32-channel gate driver, 291,600 bytes GRAM for graphic display data of 360RGBx360 dots, and power supply circuit.

GC9B71 supports parallel 8-bit data bus MCU interface, 3-/4-line serial peripheral interface (SPI) and Quad serial peripheral interface and MIPI interface. The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

GC9B71 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the GC9B71 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

1. Features

- Dual gate TFT LCD driver with 0D 0C
- Display resolution: [360 RGB] (H) x 360(V)
- Output:
  - 540 source outputs
  - 32 gate outputs
- Resolution:
  240x240：S91-S450
  320x320：S31-S510
  320x360：S31-S510
  360x360：S1-S540
  320x390：S31-S510
- a-TFT LCD driver with on-chip full display RAM: 291,600 bytes
- System Interface
  - 8-bits, MCU 8080-I
  - 8-bits, 9-bits Serial Peripheral Interface (SPI) and 2 data lane SPI
  - Quad Serial Peripheral Interface
  - MIPI（1 lane）
- Display mode:
  - Full color mode (Idle mode OFF): 16.7M-color（with dither in QSPI interface only）
  - Full color mode (Idle mode OFF): 262K-color (selectable color depth mode by software)
  - Reduce color mode (Idle mode ON): 8-color
- Power saving mode:
  - Sleep mode
- Frame rate
  -Normal mode（20Hz~65Hz）
  -Idle mode （1Hz~60Hz）
- On chip functions:
  - Timing generator
  - Oscillator
  - DC/DC converter
  - column ， dot inversion
- Low -power consumption architecture
  - Low operating power supplies:
    - VDDI = 1.65V ~ 3.3V (logic)
    - VDDB = 2.5V ~ 3.3V (analog)
- LCD Voltage drive:
  - Source/Gamma power supply voltage
    - Vreg1A ~ vreg2A = 6.5V ~-4.4V
  - Gate driver output voltage
    - VGH - GND = 8.0V ~ 15.0V
    - VGL - GND = -12.0V ~ -7.0V

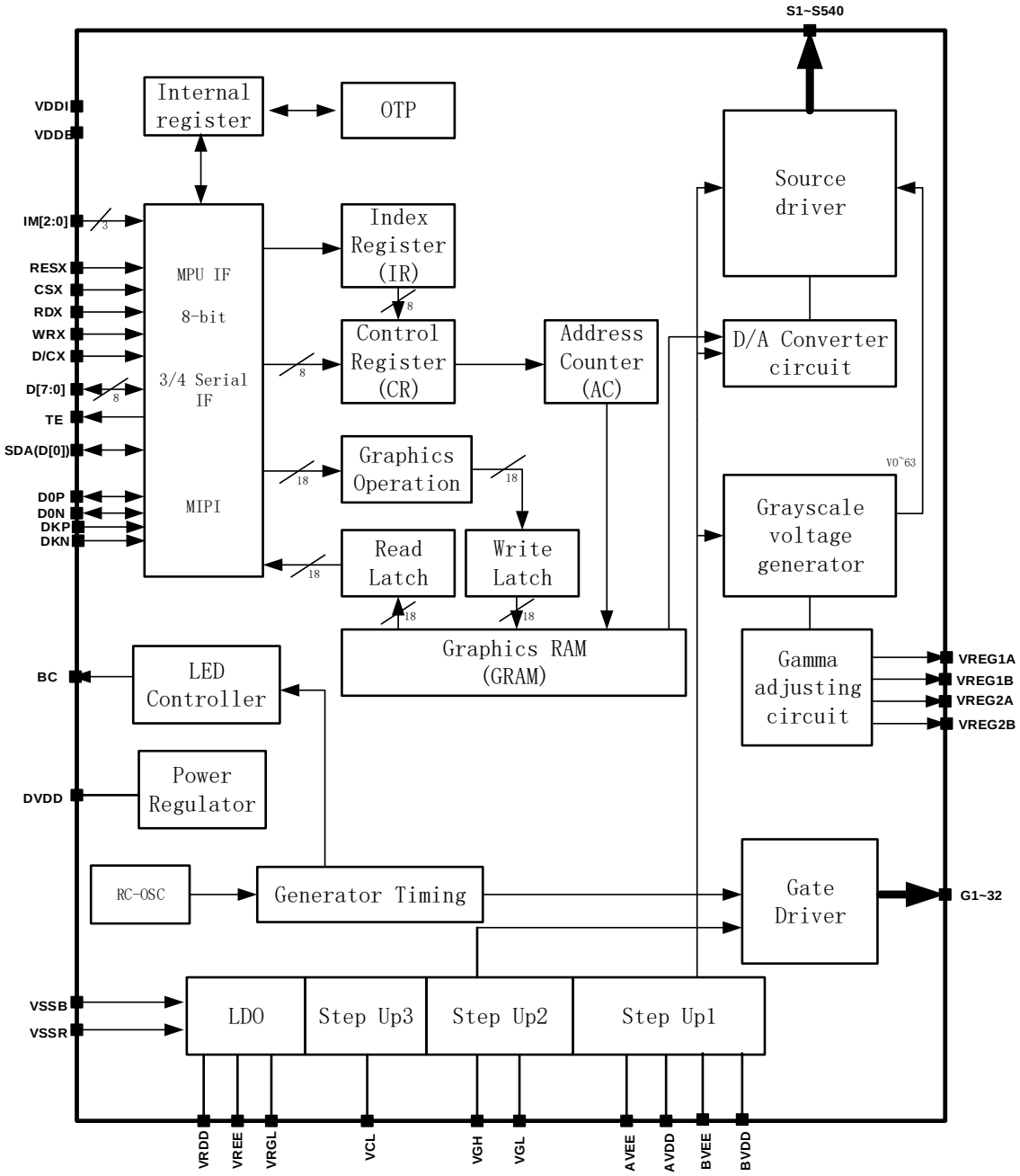
- VCOM connect to GND

◆ Operate temperature range: -40℃to 80℃

2. Block Diagram

2.1. Block diagram

Figure1



2.2. Pin Description

Table 1.

Power Supply Pins			
Pin Name	I/O	Connect Pin	Descriptions
VDDI(IOVCC)	I	VDDI	Low voltage power supply for interface logic circuits(1.65~3.3V)
VDDB(VCI)	I	VDDB	High voltage power supply for analog circuit blocks(2.5~3.3V)
VSSB/VSSR	I	GND	System ground level

Table 2

<table>
<tr><th colspan="4">Interface Logic Signals</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Connect Pin</th><th>Descriptions</th></tr>
<tr><td>IM[2:0]</td><td>I</td><td>(VDDI/ GND)</td><td>-Select the MCU interface mode
<table>
<tr><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">MCU-Interface</th><th colspan="2">Pins in use</th></tr>
<tr><th>Register</th><th>GRAM</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>8080- MCU 8bit interface I</td><td>D[7:0]</td><td>D[7:0]</td></tr>
<tr><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>QSPI</td><td>SDA/D[0]</td><td>SDA/D[0], D[3:1]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface I</td><td>SDA/D[0]</td><td>SDA/D[0]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MIPI</td><td colspan="2">D0P,D0N,DKP,DKN</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>4-wire 8-bit data serial interface I</td><td>SDA/D[0]</td><td>SDA/D[0]</td></tr>
</table>
MPU Parallel interface bus and serial interface select
Fix this pin at VDDI or GND.</td></tr>
<tr><td>RESX</td><td>I</td><td>MCU (VDDI/GND)</td><td>This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low.</td></tr>
<tr><td>CSX</td><td>I</td><td>MCU (VDDI/GND)</td><td>Chip select input pin("Low" enable).
This pin can be permanently fixed "Low" in MPU interface mode only.</td></tr>
<tr><td>D/CX (SCL)</td><td>I</td><td>MCU (VDDI/ GND)</td><td>This pin is used to select "Data or Command" in the parallel interface
When DCX='1', data is selected.
When DCX='0', command is selected.
This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit /QSPI serial interface.
If not used, this pin should be connected to VDDI or GND.</td></tr>
<tr><td>RDX</td><td>I</td><td>MCU (VDDI/ GND)</td><td>8080-I/8080-II system (RDX): Serves as a read signal and MCU read data at the rising edge.
Fix to VDDI level when not in use</td></tr>
<tr><td>WRX (D/CX)</td><td>I</td><td>MCU (VDDI/ GND)</td><td>8080-I/8080-II system (WRX): Serves as a write signal and writes data at the rising edge.
4-wire system (D/CX): Serves as command or parameter select.
3-wire 2data mode： Serves as second data pin
Fix to VDDI level when not in use.</td></tr>
<tr><td>D[7:0] D[0]/SDA</td><td>I/O</td><td>MCU (VDDI/ GND)</td><td>8-bit parallel bi-directional data bus for MCU system
When IM[2]=1, D[0]server as SDA as Serial in/out signal in 3-wire 9-bit/4-wire 8-bit/QSPI serial data interface.
In QSPI 4wire mode D[3:1] Server as SDA[3:1]
Fix to GND level when not in use</td></tr>
<tr><td>TE</td><td>O</td><td>MCU (VDDI/ GND)</td><td>Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is</td></tr>
</table>

			low. If not used, open this pin.
DKP/ Clock_P	I	MIPI	- Positive polarity of low voltage differential clock signal If MIPI are not used, they should be connected to GND.
DKN/ Clock_N	I	MIPI	- Negative polarity of low voltage differential clock signal If MIPI are not used, they should be connected to GND.
D0P/ Data_P	I/O	MIPI	- Positive polarity of low voltage differential data signal If MIPI are not used, they should be connected to GND
D0N/ Data_N	I/O	MIPI	- Negative polarity of low voltage differential data signal If MIPI are not used, they should be connected to GND
PSWAP	I	MCU(VDDI/GND)	Differential clock polarity swap For MIPI DSI interface 0: D0P->D0P, D0N->D0N; DKP->DKP, DKN->DKN, 1: D0P->D0N, D0N->D0P; DKP->DKN, DKN->DKP,
VCOM	I	GND	Fix to GND
TESTP	O	OPEN	Test pin
TESTN	O	OPEN	Test pin

Note:

1. If CSX is connected to GND in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Further more there will be no influence to the Power Consumption of the display module.

2. When CSX='1', there is no influence to the parallel and serial interface.

Table 3

LCD Driver Input/Output Pins			
Pin Name	I/O	Connect Pin	Descriptions
S540~S1	O	LCD	Source output signals. Leave the pin to open when not in use.
G1~G32	O	LCD	Gate output signals. Leave the pin to open when not in use.
VCOM	O	GND	Connect to GND.
VRDD	O	Power	Power supply for AVDD.
VREE	O	Power	Power supply for AVEE.
DVDD	O	Power	Regulated Low voltage level for interface circuits Don't apply any external power to this pin
VRGL	O	Power	Power supply for VCL.
AVDD	O	Power	Analog power for Source.
AVEE	O	Power	Analog power for Source.
VGH	O	Power	Power supply for the gate driver(Positive).
VGL	O	Power	Power supply for the gate driver(Negative).
VREG1A	O	Ref	VREG1A is the highest positive grayscale reference voltage of source driver.
VREG1B	O	Ref	VREG1B is the lowest positive grayscale reference voltage of source driver. test by VREGP pin
VREG2B	O	Ref	VREG2B is the lowest negative grayscale reference voltage of source driver, test by VREGP pin
VREG2A	O	Ref	VREG2A is the highest negative grayscale reference voltage of source driver , test VREGN pin
BC	O	Dig IO	Output pin for PWM (Pulse width Modulation) signal of LED driving. If not used, open this pin.

Table 4

Test Pins			
Pin Name	I/O	Connect Pin	Descriptions
OSC_IN	I/O	Open	Test pin
OSC_TEST	I/O	Open	Test pin
VPP	I/O	Open	Test pin
DUMMY	-	Open	Input pads used only for test purpose at IC-side. During normal operation , leave these pads open.

Liquid crystal power supply specifications Table

Table 5

No.	Item		Description
1	TFT Source Driver		support 360*RGB（max）
2	TFT Gate Driver		32 pins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1~S540	V0~V63 grayscales
		G1~G32	VGH-VGL
5	Input Voltage	VDDI	1.65~3.30V
		VDDB	2.50~3.30V
6	Liquid Crystal Drive Voltages	AVDD	6.5~7.5V
		AVEE	-5.5V~-4.5V
		VGH	8.0~15.0V
		VGL	-11.0~-7.0V
		VCL	-3.0~-1.5V
7	Internal Step-up Circuits	AVDD	VDDB*3
		AVEE	VDDB*-2
		VGH	VDDB*5
		VGL	VDDB*-5
		VCL	VDDB*-1

2.3.PAD coordinates

NO.	Text Name	X	Y	NO.	Text Name	X	Y	NO.	Text Name	X	Y
1	VSSB	-5974	-397	51	S<7>	-4085	-307	101	S<57>	-3385	-307
2	VSSB	-5929	-397	52	S<8>	-4071	-417	102	S<58>	-3371	-417
3	VSSB	-5884	-397	53	S<9>	-4057	-307	103	S<59>	-3357	-307
4	VDDB	-5839	-397	54	S<10>	-4043	-417	104	S<60>	-3343	-417
5	VDDB	-5794	-397	55	S<11>	-4029	-307	105	S<61>	-3329	-307
6	VDDB	-5749	-397	56	S<12>	-4015	-417	106	S<62>	-3315	-417
7	VDDI	-5704	-397	57	S<13>	-4001	-307	107	S<63>	-3301	-307
8	VDDI	-5659	-397	58	S<14>	-3987	-417	108	S<64>	-3287	-417
9	TE	-5614	-397	59	S<15>	-3973	-307	109	S<65>	-3273	-307
10	RD	-5569	-397	60	S<16>	-3959	-417	110	S<66>	-3259	-417
11	DC	-5524	-397	61	S<17>	-3945	-307	111	S<67>	-3245	-307
12	CS	-5479	-397	62	S<18>	-3931	-417	112	S<68>	-3231	-417
13	WR	-5434	-397	63	S<19>	-3917	-307	113	S<69>	-3217	-307
14	BC	-5389	-397	64	S<20>	-3903	-417	114	S<70>	-3203	-417
15	DB<0>	-5344	-397	65	S<21>	-3889	-307	115	S<71>	-3189	-307
16	DB<1>	-5299	-397	66	S<22>	-3875	-417	116	S<72>	-3175	-417
17	DB<2>	-5254	-397	67	S<23>	-3861	-307	117	S<73>	-3161	-307
18	DB<3>	-5209	-397	68	S<24>	-3847	-417	118	S<74>	-3147	-417
19	DB<4>	-5164	-397	69	S<25>	-3833	-307	119	S<75>	-3133	-307
20	DB<5>	-5119	-397	70	S<26>	-3819	-417	120	S<76>	-3119	-417
21	DB<6>	-5074	-397	71	S<27>	-3805	-307	121	S<77>	-3105	-307
22	DB<7>	-5029	-397	72	S<28>	-3791	-417	122	S<78>	-3091	-417
23	TESTP	-4984	-397	73	S<29>	-3777	-307	123	S<79>	-3077	-307
24	TESTN	-4939	-397	74	S<30>	-3763	-417	124	S<80>	-3063	-417
25	Align mark	-4861	-374	75	S<31>	-3749	-307	125	S<81>	-3049	-307
26	GOUT<32>	-4790.5	-397	76	S<32>	-3735	-417	126	S<82>	-3035	-417
27	GOUT<31>	-4758.5	-397	77	S<33>	-3721	-307	127	S<83>	-3021	-307
28	GOUT<30>	-4726.5	-397	78	S<34>	-3707	-417	128	S<84>	-3007	-417
29	GOUT<29>	-4694.5	-397	79	S<35>	-3693	-307	129	S<85>	-2993	-307
30	GOUT<28>	-4662.5	-397	80	S<36>	-3679	-417	130	S<86>	-2979	-417
31	GOUT<27>	-4630.5	-397	81	S<37>	-3665	-307	131	S<87>	-2965	-307
32	GOUT<26>	-4598.5	-397	82	S<38>	-3651	-417	132	S<88>	-2951	-417
33	GOUT<25>	-4566.5	-397	83	S<39>	-3637	-307	133	S<89>	-2937	-307
34	GOUT<24>	-4534.5	-397	84	S<40>	-3623	-417	134	S<90>	-2923	-417
35	GOUT<23>	-4502.5	-397	85	S<41>	-3609	-307	135	S<91>	-2909	-307
36	GOUT<22>	-4470.5	-397	86	S<42>	-3595	-417	136	S<92>	-2895	-417
37	GOUT<21>	-4438.5	-397	87	S<43>	-3581	-307	137	S<93>	-2881	-307
38	GOUT<20>	-4406.5	-397	88	S<44>	-3567	-417	138	S<94>	-2867	-417
39	GOUT<19>	-4374.5	-397	89	S<45>	-3553	-307	139	S<95>	-2853	-307
40	GOUT<18>	-4342.5	-397	90	S<46>	-3539	-417	140	S<96>	-2839	-417
41	GOUT<17>	-4310.5	-397	91	S<47>	-3525	-307	141	S<97>	-2825	-307
42	DUM	-4211	-417	92	S<48>	-3511	-417	142	S<98>	-2811	-417
43	DUM	-4197	-307	93	S<49>	-3497	-307	143	S<99>	-2797	-307
44	DUM	-4183	-417	94	S<50>	-3483	-417	144	S<100>	-2783	-417
45	S<1>	-4169	-307	95	S<51>	-3469	-307	145	S<101>	-2769	-307
46	S<2>	-4155	-417	96	S<52>	-3455	-417	146	S<102>	-2755	-417
47	S<3>	-4141	-307	97	S<53>	-3441	-307	147	S<103>	-2741	-307
48	S<4>	-4127	-417	98	S<54>	-3427	-417	148	S<104>	-2727	-417
49	S<5>	-4113	-307	99	S<55>	-3413	-307	149	S<105>	-2713	-307
50	S<6>	-4099	-417	100	S<56>	-3399	-417	150	S<106>	-2699	-417

NO.	Text Name	X	Y	NO.	Text Name	X	Y	NO.	Text Name	X	Y
151	S<107>	-268	-307	201	S<157>	-198	-307	251	S<207>	-1285	-307
152	S<108>	-267	-417	202	S<158>	-197	-417	252	S<208>	-1271	-417
153	S<109>	-265	-307	203	S<159>	-195	-307	253	S<209>	-1257	-307
154	S<110>	-264	-417	204	S<160>	-194	-417	254	S<210>	-1243	-417
155	S<111>	-262	-307	205	S<161>	-192	-307	255	S<211>	-1229	-307
156	S<112>	-261	-417	206	S<162>	-191	-417	256	S<212>	-1215	-417
157	S<113>	-260	-307	207	S<163>	-190	-307	257	S<213>	-1201	-307
158	S<114>	-258	-417	208	S<164>	-188	-417	258	S<214>	-1187	-417
159	S<115>	-257	-307	209	S<165>	-187	-307	259	S<215>	-1173	-307
160	S<116>	-255	-417	210	S<166>	-185	-417	260	S<216>	-1159	-417
161	S<117>	-254	-307	211	S<167>	-184	-307	261	S<217>	-1145	-307
162	S<118>	-253	-417	212	S<168>	-183	-417	262	S<218>	-1131	-417
163	S<119>	-251	-307	213	S<169>	-181	-307	263	S<219>	-1117	-307
164	S<120>	-250	-417	214	S<170>	-180	-417	264	S<220>	-1103	-417
165	S<121>	-248	-307	215	S<171>	-178	-307	265	S<221>	-1089	-307
166	S<122>	-247	-417	216	S<172>	-177	-417	266	S<222>	-1075	-417
167	S<123>	-246	-307	217	S<173>	-176	-307	267	S<223>	-1061	-307
168	S<124>	-244	-417	218	S<174>	-174	-417	268	S<224>	-1047	-417
169	S<125>	-243	-307	219	S<175>	-173	-307	269	S<225>	-1033	-307
170	S<126>	-241	-417	220	S<176>	-171	-417	270	S<226>	-1019	-417
171	S<127>	-240	-307	221	S<177>	-170	-307	271	S<227>	-1005	-307
172	S<128>	-239	-417	222	S<178>	-169	-417	272	S<228>	-991	-417
173	S<129>	-237	-307	223	S<179>	-167	-307	273	S<229>	-977	-307
174	S<130>	-236	-417	224	S<180>	-166	-417	274	S<230>	-963	-417
175	S<131>	-234	-307	225	S<181>	-164	-307	275	S<231>	-949	-307
176	S<132>	-233	-417	226	S<182>	-163	-417	276	S<232>	-935	-417
177	S<133>	-232	-307	227	S<183>	-162	-307	277	S<233>	-921	-307
178	S<134>	-230	-417	228	S<184>	-160	-417	278	S<234>	-907	-417
179	S<135>	-229	-307	229	S<185>	-159	-307	279	S<235>	-893	-307
180	S<136>	-227	-417	230	S<186>	-157	-417	280	S<236>	-879	-417
181	S<137>	-226	-307	231	S<187>	-156	-307	281	S<237>	-865	-307
182	S<138>	-225	-417	232	S<188>	-155	-417	282	S<238>	-851	-417
183	S<139>	-223	-307	233	S<189>	-153	-307	283	S<239>	-837	-307
184	S<140>	-222	-417	234	S<190>	-152	-417	284	S<240>	-823	-417
185	S<141>	-220	-307	235	S<191>	-150	-307	285	S<241>	-809	-307
186	S<142>	-219	-417	236	S<192>	-149	-417	286	S<242>	-795	-417
187	S<143>	-218	-307	237	S<193>	-148	-307	287	S<243>	-781	-307
188	S<144>	-216	-417	238	S<194>	-146	-417	288	S<244>	-767	-417
189	S<145>	-215	-307	239	S<195>	-145	-307	289	S<245>	-753	-307
190	S<146>	-213	-417	240	S<196>	-143	-417	290	S<246>	-739	-417
191	S<147>	-212	-307	241	S<197>	-142	-307	291	S<247>	-725	-307
192	S<148>	-211	-417	242	S<198>	-141	-417	292	S<248>	-711	-417
193	S<149>	-209	-307	243	S<199>	-139	-307	293	S<249>	-697	-307
194	S<150>	-208	-417	244	S<200>	-138	-417	294	S<250>	-683	-417
195	S<151>	-206	-307	245	S<201>	-136	-307	295	S<251>	-669	-307
196	S<152>	-205	-417	246	S<202>	-135	-417	296	S<252>	-655	-417
197	S<153>	-204	-307	247	S<203>	-134	-307	297	S<253>	-641	-307
198	S<154>	-202	-417	248	S<204>	-132	-417	298	S<254>	-627	-417
199	S<155>	-201	-307	249	S<205>	-131	-307	299	S<255>	-613	-307
200	S<156>	-199	-417	250	S<206>	-129	-417	300	S<256>	-599	-417

NO.	Text Name	X	Y	NO.	Text Name	X	Y	NO.	Text Name	X	Y
301	S<257>	-585	-307	351	S<297>	767	-417	401	S<347>	1467	-417
302	S<258>	-571	-417	352	S<298>	781	-307	402	S<348>	1481	-307
303	S<259>	-557	-307	353	S<299>	795	-417	403	S<349>	1495	-417
304	S<260>	-543	-417	354	S<300>	809	-307	404	S<350>	1509	-307
305	S<261>	-529	-307	355	S<301>	823	-417	405	S<351>	1523	-417
306	S<262>	-515	-417	356	S<302>	837	-307	406	S<352>	1537	-307
307	S<263>	-501	-307	357	S<303>	851	-417	407	S<353>	1551	-417
308	S<264>	-487	-417	358	S<304>	865	-307	408	S<354>	1565	-307
309	S<265>	-473	-307	359	S<305>	879	-417	409	S<355>	1579	-417
310	S<266>	-459	-417	360	S<306>	893	-307	410	S<356>	1593	-307
311	S<267>	-445	-307	361	S<307>	907	-417	411	S<357>	1607	-417
312	S<268>	-431	-417	362	S<308>	921	-307	412	S<358>	1621	-307
313	S<269>	-417	-307	363	S<309>	935	-417	413	S<359>	1635	-417
314	S<270>	-403	-417	364	S<310>	949	-307	414	S<360>	1649	-307
315	DUM	-389	-307	365	S<311>	963	-417	415	S<361>	1663	-417
316	DUM	-375	-417	366	S<312>	977	-307	416	S<362>	1677	-307
317	DUM	-349	-417	367	S<313>	991	-417	417	S<363>	1691	-417
318	AVDD	-323	-417	368	S<314>	1005	-307	418	S<364>	1705	-307
319	DUM	-297	-417	369	S<315>	1019	-417	419	S<365>	1719	-417
320	BVEE	297	-417	370	S<316>	1033	-307	420	S<366>	1733	-307
321	DUM	323	-417	371	S<317>	1047	-417	421	S<367>	1747	-417
322	BVDD	349	-417	372	S<318>	1061	-307	422	S<368>	1761	-307
323	DUM	375	-417	373	S<319>	1075	-417	423	S<369>	1775	-417
324	DUM	389	-307	374	S<320>	1089	-307	424	S<370>	1789	-307
325	S<271>	403	-417	375	S<321>	1103	-417	425	S<371>	1803	-417
326	S<272>	417	-307	376	S<322>	1117	-307	426	S<372>	1817	-307
327	S<273>	431	-417	377	S<323>	1131	-417	427	S<373>	1831	-417
328	S<274>	445	-307	378	S<324>	1145	-307	428	S<374>	1845	-307
329	S<275>	459	-417	379	S<325>	1159	-417	429	S<375>	1859	-417
330	S<276>	473	-307	380	S<326>	1173	-307	430	S<376>	1873	-307
331	S<277>	487	-417	381	S<327>	1187	-417	431	S<377>	1887	-417
332	S<278>	501	-307	382	S<328>	1201	-307	432	S<378>	1901	-307
333	S<279>	515	-417	383	S<329>	1215	-417	433	S<379>	1915	-417
334	S<280>	529	-307	384	S<330>	1229	-307	434	S<380>	1929	-307
335	S<281>	543	-417	385	S<331>	1243	-417	435	S<381>	1943	-417
336	S<282>	557	-307	386	S<332>	1257	-307	436	S<382>	1957	-307
337	S<283>	571	-417	387	S<333>	1271	-417	437	S<383>	1971	-417
338	S<284>	585	-307	388	S<334>	1285	-307	438	S<384>	1985	-307
339	S<285>	599	-417	389	S<335>	1299	-417	439	S<385>	1999	-417
340	S<286>	613	-307	390	S<336>	1313	-307	440	S<386>	2013	-307
341	S<287>	627	-417	391	S<337>	1327	-417	441	S<387>	2027	-417
342	S<288>	641	-307	392	S<338>	1341	-307	442	S<388>	2041	-307
343	S<289>	655	-417	393	S<339>	1355	-417	443	S<389>	2055	-417
344	S<290>	669	-307	394	S<340>	1369	-307	444	S<390>	2069	-307
345	S<291>	683	-417	395	S<341>	1383	-417	445	S<391>	2083	-417
346	S<292>	697	-307	396	S<342>	1397	-307	446	S<392>	2097	-307
347	S<293>	711	-417	397	S<343>	1411	-417	447	S<393>	2111	-417
348	S<294>	725	-307	398	S<344>	1425	-307	448	S<394>	2125	-307
349	S<295>	739	-417	399	S<345>	1439	-417	449	S<395>	2139	-417
350	S<296>	753	-307	400	S<346>	1453	-307	450	S<396>	2153	-307

NO.	Text Name	X	Y	NO.	Text Name	X	Y	NO.	Text Name	X	Y
451	S<397>	2167	-417	501	S<447>	2867	-417	551	S<497>	3567	-417
452	S<398>	2181	-307	502	S<448>	2881	-307	552	S<498>	3581	-307
453	S<399>	2195	-417	503	S<449>	2895	-417	553	S<499>	3595	-417
454	S<400>	2209	-307	504	S<450>	2909	-307	554	S<500>	3609	-307
455	S<401>	2223	-417	505	S<451>	2923	-417	555	S<501>	3623	-417
456	S<402>	2237	-307	506	S<452>	2937	-307	556	S<502>	3637	-307
457	S<403>	2251	-417	507	S<453>	2951	-417	557	S<503>	3651	-417
458	S<404>	2265	-307	508	S<454>	2965	-307	558	S<504>	3665	-307
459	S<405>	2279	-417	509	S<455>	2979	-417	559	S<505>	3679	-417
460	S<406>	2293	-307	510	S<456>	2993	-307	560	S<506>	3693	-307
461	S<407>	2307	-417	511	S<457>	3007	-417	561	S<507>	3707	-417
462	S<408>	2321	-307	512	S<458>	3021	-307	562	S<508>	3721	-307
463	S<409>	2335	-417	513	S<459>	3035	-417	563	S<509>	3735	-417
464	S<410>	2349	-307	514	S<460>	3049	-307	564	S<510>	3749	-307
465	S<411>	2363	-417	515	S<461>	3063	-417	565	S<511>	3763	-417
466	S<412>	2377	-307	516	S<462>	3077	-307	566	S<512>	3777	-307
467	S<413>	2391	-417	517	S<463>	3091	-417	567	S<513>	3791	-417
468	S<414>	2405	-307	518	S<464>	3105	-307	568	S<514>	3805	-307
469	S<415>	2419	-417	519	S<465>	3119	-417	569	S<515>	3819	-417
470	S<416>	2433	-307	520	S<466>	3133	-307	570	S<516>	3833	-307
471	S<417>	2447	-417	521	S<467>	3147	-417	571	S<517>	3847	-417
472	S<418>	2461	-307	522	S<468>	3161	-307	572	S<518>	3861	-307
473	S<419>	2475	-417	523	S<469>	3175	-417	573	S<519>	3875	-417
474	S<420>	2489	-307	524	S<470>	3189	-307	574	S<520>	3889	-307
475	S<421>	2503	-417	525	S<471>	3203	-417	575	S<521>	3903	-417
476	S<422>	2517	-307	526	S<472>	3217	-307	576	S<522>	3917	-307
477	S<423>	2531	-417	527	S<473>	3231	-417	577	S<523>	3931	-417
478	S<424>	2545	-307	528	S<474>	3245	-307	578	S<524>	3945	-307
479	S<425>	2559	-417	529	S<475>	3259	-417	579	S<525>	3959	-417
480	S<426>	2573	-307	530	S<476>	3273	-307	580	S<526>	3973	-307
481	S<427>	2587	-417	531	S<477>	3287	-417	581	S<527>	3987	-417
482	S<428>	2601	-307	532	S<478>	3301	-307	582	S<528>	4001	-307
483	S<429>	2615	-417	533	S<479>	3315	-417	583	S<529>	4015	-417
484	S<430>	2629	-307	534	S<480>	3329	-307	584	S<530>	4029	-307
485	S<431>	2643	-417	535	S<481>	3343	-417	585	S<531>	4043	-417
486	S<432>	2657	-307	536	S<482>	3357	-307	586	S<532>	4057	-307
487	S<433>	2671	-417	537	S<483>	3371	-417	587	S<533>	4071	-417
488	S<434>	2685	-307	538	S<484>	3385	-307	588	S<534>	4085	-307
489	S<435>	2699	-417	539	S<485>	3399	-417	589	S<535>	4099	-417
490	S<436>	2713	-307	540	S<486>	3413	-307	590	S<536>	4113	-307
491	S<437>	2727	-417	541	S<487>	3427	-417	591	S<537>	4127	-417
492	S<438>	2741	-307	542	S<488>	3441	-307	592	S<538>	4141	-307
493	S<439>	2755	-417	543	S<489>	3455	-417	593	S<539>	4155	-417
494	S<440>	2769	-307	544	S<490>	3469	-307	594	S<540>	4169	-307
495	S<441>	2783	-417	545	S<491>	3483	-417	595	DUM	4183	-417
496	S<442>	2797	-307	546	S<492>	3497	-307	596	DUM	4197	-307
497	S<443>	2811	-417	547	S<493>	3511	-417	597	DUM	4211	-417
498	S<444>	2825	-307	548	S<494>	3525	-307	598	GOUT<16>	4310.5	-397
499	S<445>	2839	-417	549	S<495>	3539	-417	599	GOUT<15>	4342.5	-397
500	S<446>	2853	-307	550	S<496>	3553	-307	600	GOUT<14>	4374.5	-397

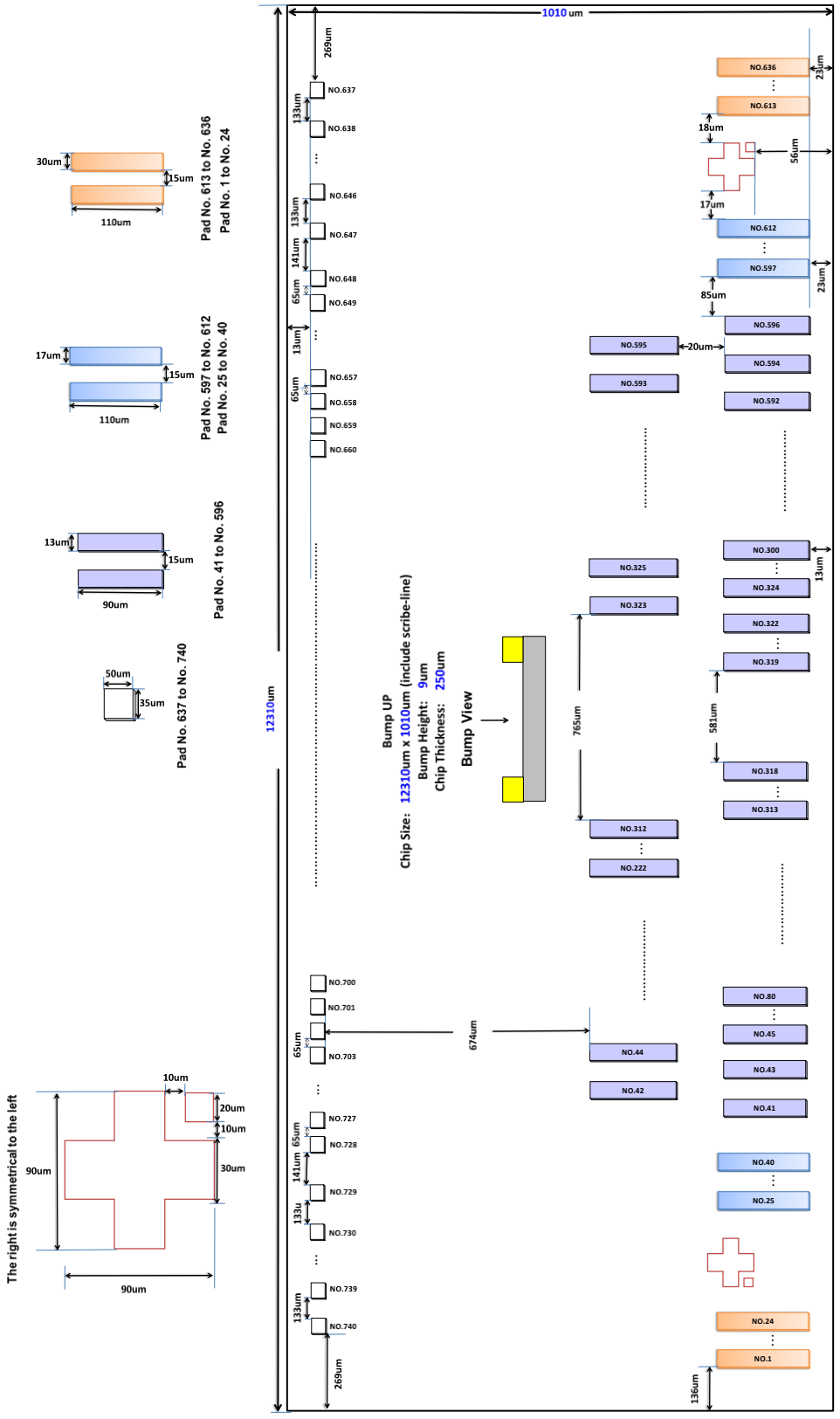
NO.	Text Name	X	Y
601	GOUT<13>	4406.5	-397
602	GOUT<12>	4438.5	-397
603	GOUT<11>	4470.5	-397
604	GOUT<10>	4502.5	-397
605	GOUT<9>	4534.5	-397
606	GOUT<8>	4566.5	-397
607	GOUT<7>	4598.5	-397
608	GOUT<6>	4630.5	-397
609	GOUT<5>	4662.5	-397
610	GOUT<4>	4694.5	-397
611	GOUT<3>	4726.5	-397
612	GOUT<2>	4758.5	-397
613	GOUT<1>	4790.5	-397
614	Align mark	4861	-374
615	VGLO	4939	-397
616	VGL	4984	-397
617	IM<2>	5029	-397
618	IM<1>	5074	-397
619	IM<0>	5119	-397
620	PSWAP	5164	-397
621	RST	5209	-397
622	VGH	5254	-397
623	VDDI	5299	-397
624	VSSB	5344	-397
625	DON	5389	-397
626	DOP	5434	-397
627	VSSB	5479	-397
628	DKN	5524	-397
629	DKP	5569	-397
630	VSSB	5614	-397
631	VSSR	5659	-397
632	VSSR	5704	-397
633	VDDB	5749	-397
634	VDDB	5794	-397
635	VDDB	5839	-397
636	VSSB	5884	-397
637	VSSB	5929	-397
638	VSSB	5974	-397
639	DUMMY	5838	437
640	DUMMY	5670	437
641	DUMMY	5502	437
642	DUMMY	5334	437
643	DUMMY	5166	437
644	DUMMY	4998	437
645	DUMMY	4830	437
646	DUMMY	4662	437
647	DUMMY	4494	437
648	DUMMY	4326	437
649	DUMMY	4150	437
650	DUMMY	4050	437

NO.	Text Name	X	Y
651	DUMMY	3950	437
652	DUMMY	3850	437
653	DUMMY	3750	437
654	DUMMY	3650	437
655	DUMMY	3550	437
656	DUMMY	3450	437
657	DUMMY	3350	437
658	DUMMY	3250	437
659	DUMMY	3150	437
660	DUMMY	3050	437
661	DUMMY	2950	437
662	DUMMY	2850	437
663	DUMMY	2750	437
664	DUMMY	2650	437
665	DUMMY	2550	437
666	DUMMY	2450	437
667	DUMMY	2350	437
668	DUMMY	2250	437
669	DUMMY	2150	437
670	DUMMY	2050	437
671	DUMMY	1950	437
672	DUMMY	1850	437
673	DUMMY	1750	437
674	DUMMY	1650	437
675	DUMMY	1550	437
676	DUMMY	1450	437
677	DUMMY	1350	437
678	DUMMY	1250	437
679	DUMMY	1150	437
680	DUMMY	1050	437
681	DUMMY	950	437
682	DUMMY	850	437
683	DUMMY	750	437
684	DUMMY	650	437
685	DUMMY	550	437
686	DUMMY	450	437
687	DUMMY	350	437
688	DUMMY	250	437
689	DUMMY	150	437
690	DUMMY	50	437
691	DUMMY	-50	437
692	DUMMY	-150	437
693	DUMMY	-250	437
694	DUMMY	-350	437
695	DUMMY	-450	437
696	DUMMY	-550	437
697	DUMMY	-650	437
698	DUMMY	-750	437
699	DUMMY	-850	437
700	DUMMY	-950	437

NO.	Text Name	X	Y
701	DUMMY	-1050	437
702	DUMMY	-1150	437
703	DUMMY	-1250	437
704	DUMMY	-1350	437
705	DUMMY	-1450	437
706	DUMMY	-1550	437
707	VPP	-1650	437
708	VREG1A	-1750	437
709	VREGP	-1850	437
710	VREG_VREF	-1950	437
711	DUMMY	-2050	437
712	DUMMY	-2150	437
713	DUMMY	-2250	437
714	DUMMY	-2350	437
715	DUMMY	-2450	437
716	DUMMY	-2550	437
717	DUMMY	-2650	437
718	DUMMY	-2750	437
719	VREGN	-2850	437
720	DUMMY	-2950	437
721	OSC_OUT	-3050	437
722	OSC_IN	-3150	437
723	DUMMY	-3250	437
724	DUMMY	-3350	437
725	DUMMY	-3450	437
726	DUMMY	-3550	437
727	DUMMY	-3650	437
728	DUMMY	-3750	437
729	DUMMY	-3850	437
730	DUMMY	-3950	437
731	DUMMY	-4050	437
732	DUMMY	-4150	437
733	DUMMY	-4326	437
734	DUMMY	-4494	437
735	DUMMY	-4662	437
736	DUMMY	-4830	437
737	DUMMY	-4998	437
738	DUMMY	-5166	437
739	DUMMY	-5334	437
740	DUMMY	-5502	437
741	DUMMY	-5670	437
742	DUMMY	-5838	437

Name	X-axis	Y-axis
left mark	-4861	-374
right mark	4861	-374

Chip Size (include scribe line): 12310um x 1010um
Chip thickness: 250um
Bump height: 9um



3. Interface setting

3.1. MCU interfaces

GC9B71 provides the 8-bit parallel system interface for 8080-I, and 3-/4-line serial system interface for serial data input, QSPI and MIPI interface. The input system interface is selected by external pins IM [2:0] and the bit formal per pixel color order is selected by DBI [2:0] 3-bits of 3Ah register.

3.1.1.MCU interface selection

The selection of interface is done by setting external pins IM [2:0] as shown in the following table.

Table 6

IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
				Register/Content	GRAM
0	0	0	8080- MCU 8bit bus interface I	D[7: 0]	D[7: 0] , WRX,RDX,CSX,D/CX
0	X	X	X	X	X
1	0	0	Quad serial interface	SDA/D[0]	SDA/D[0], D[3:1],CLK,CSX
1	0	1	3-wire 9-bit data serial interface I	SDA/D[0]	SCL, SDA/D[0], CSX
1	1	0	MIPI	D0P, D0N, DKP, DKN	
1	1	1	4-wire 8-bit data serial interface I	SDA/D[0]	SCL, SDA/D[0], D/CX, CSX

3.1.2.8080-I Series Parallel Interface

GC9B71 can be accessed via 8-bit MCU 8080-I series parallel interface. The chip select CSX (active low) is used to enable or disable GC9B71 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[7:0] is parallel data bus.

GC9B71 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [7:0] bits are display RAM data or command's parameters. When D/CX='0', D[7:0] bits are commands.

The 8080-I series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The selection of 8080-I series parallel interface is shown as the table in the following.

Table 7

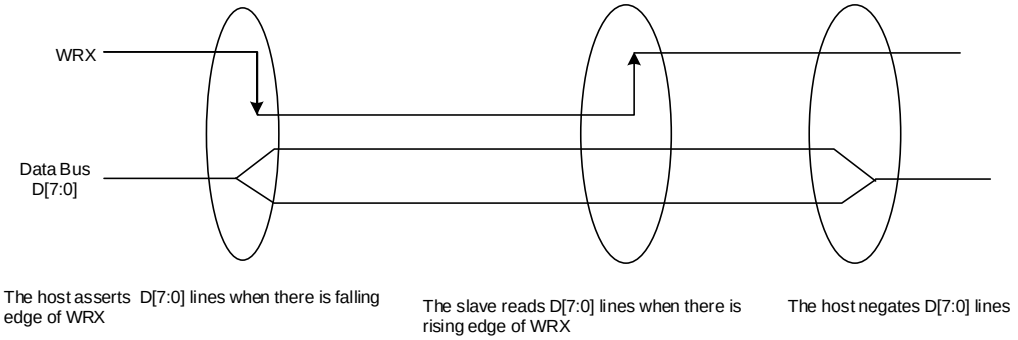
IM2	IM1	IM0	MCU-Interface	CSX	WRX	RDX	D/CX	Function
0	0	0	8080 MCU 8-bit bus interface I	"L"	↑	"H"	"L"	Write command code.
				"L"	"H"	↑	"H"	Read internal status.
				"L"	↑	"H"	"H"	Write parameter or display data.
				"L"	"H"	↑	"H"	Reads parameter or display data.

3.1.3.Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is SRAM data or command's parameter.

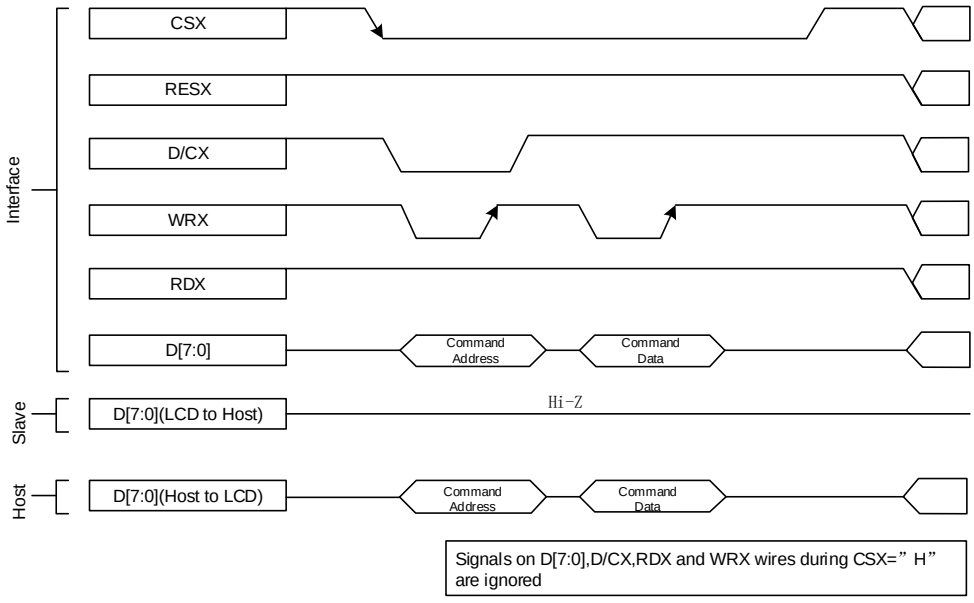
The following figure shows a write cycle for the 8080-I MCU interface.

Figure 2.



Note: WRX is an unsynchronized signal (It can be stopped)

Figure 3.

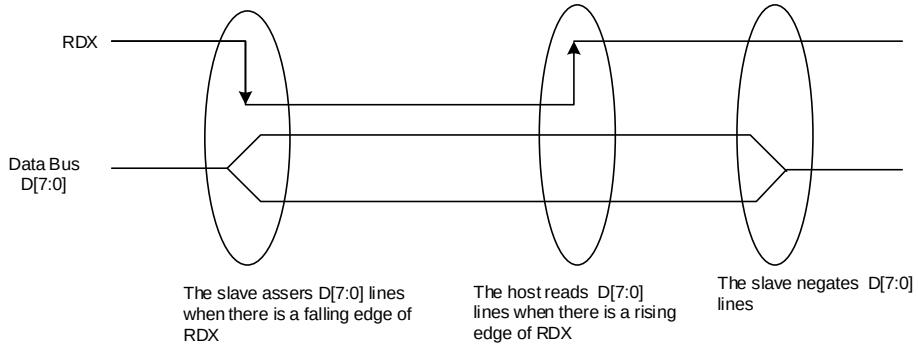


3.1.4.Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle, while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

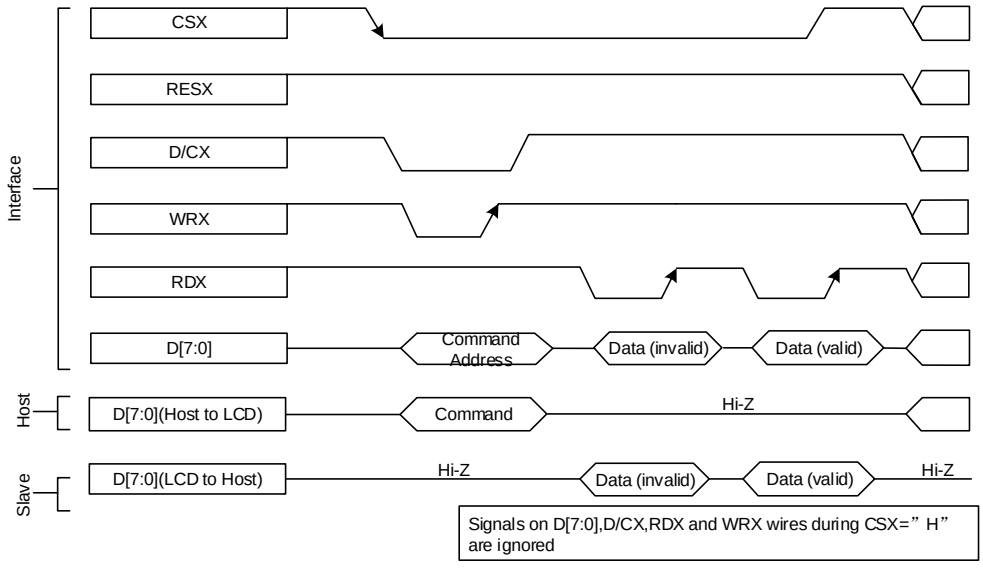
The following figure shows the read cycle for the 8080-I MCU interface.

Figure 4.



Note: RDX is an unsynchronized signal (It can be stopped).

Figure 5.



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

3.1.5.Serial Interface

The selection of interface is done by IM [2:0] bits. Please refer to the Table in the following.

Table 8.

IM2	IM1	IM0	MCU-Interface Mode	CSX	D/CX	SCL	Function
1	0	1	3-line serial interface I	“L”	-		Read/Write command, parameter or display data.
1	1	1	4-line serial interface I	“L”	"H/L"		Read/Write command, parameter or display data.

GC9B71 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and GC9B71. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA). The 4-line serial mode consists of the Data/ Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA) for data transmission. The data bus (D [7:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

3.1.6.Write Cycle Sequence

The write mode of the interface means that host writes commands or data to GC9B71. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is “low”, the transmission byte is interpreted as a command byte. If the D/CX bit is “high”, the transmission byte is stored as the display data RAM(Memory write command),or command register as parameter.

Any instruction can be sent in any order to GC9B71 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

Figure 10.

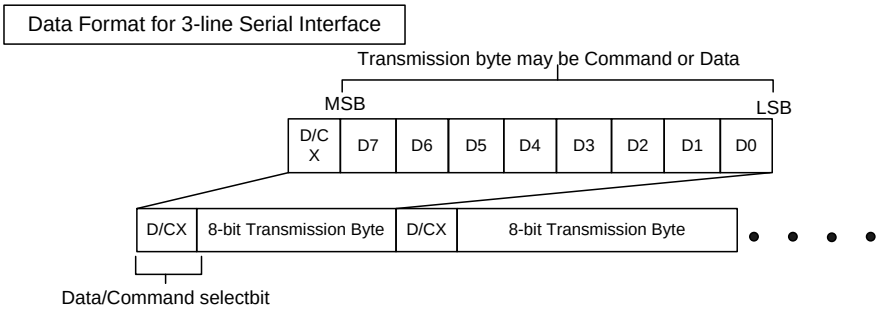
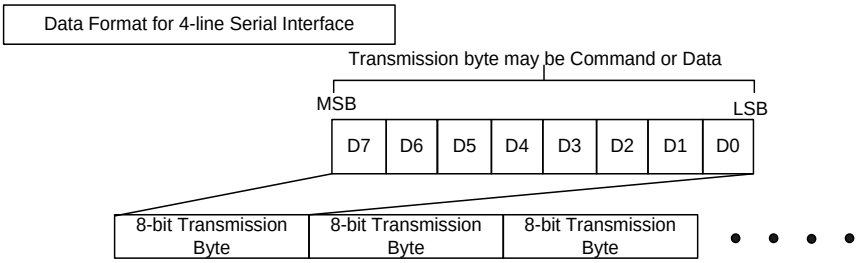


Figure11.



Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by GC9B71 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

Figure 12.

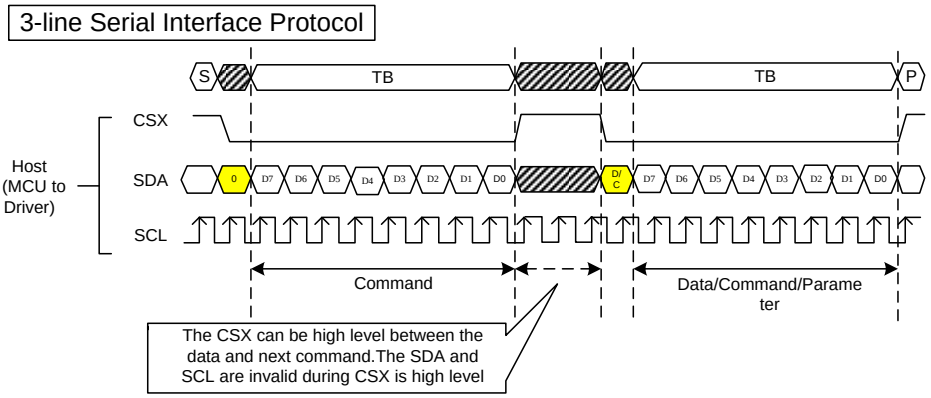
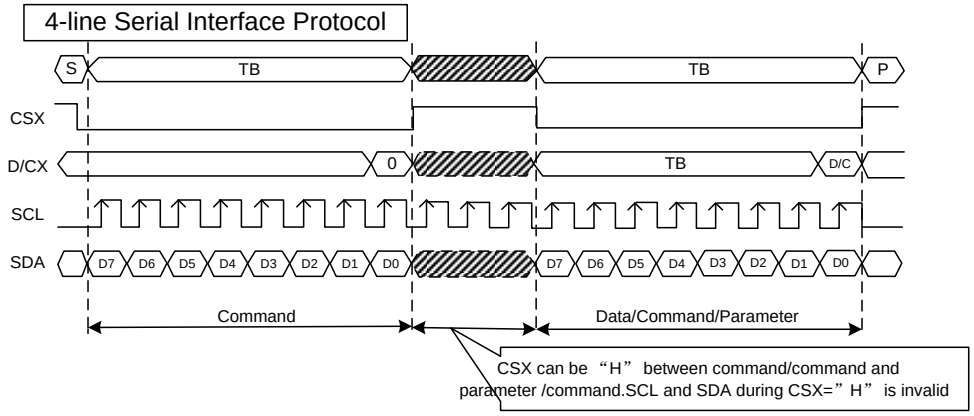


Figure 13.



3.1.7.Read Cycle Sequence

The read mode of interface means that the host reads register's parameter from GC9B71. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. GC9B71 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

Figure 14.

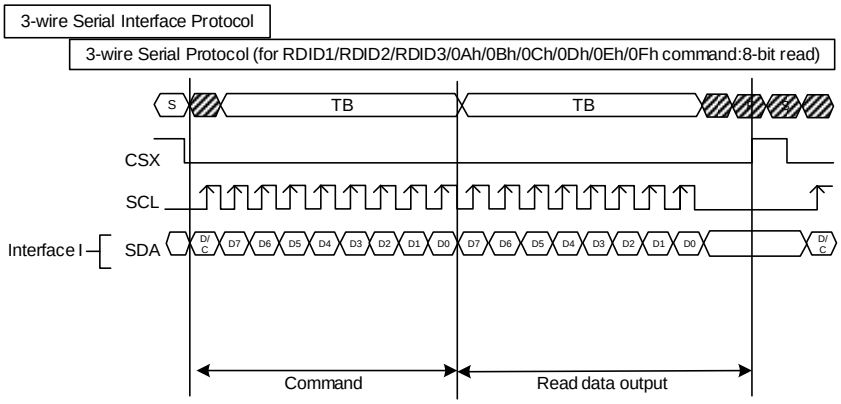


Figure 15.

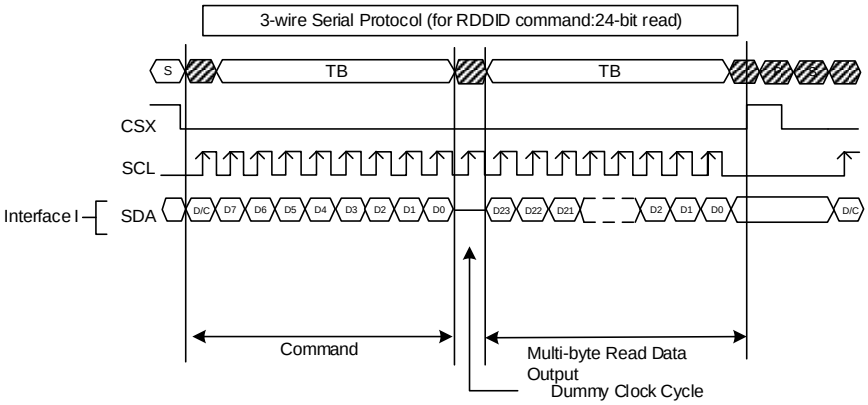


Figure 16.

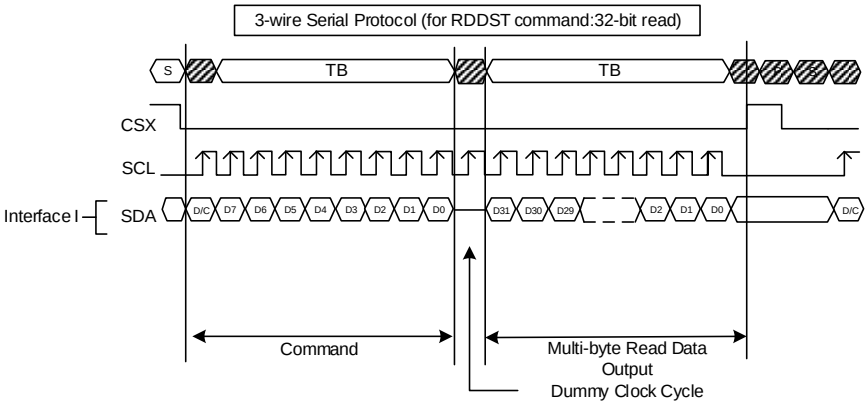


Figure 17.

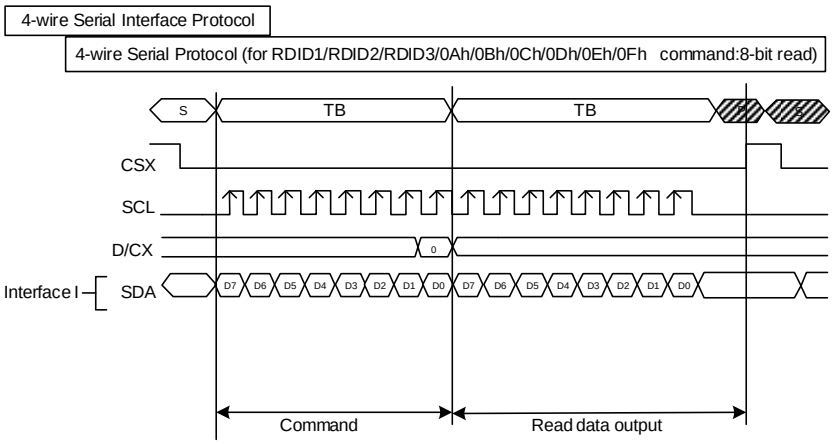


Figure 18.

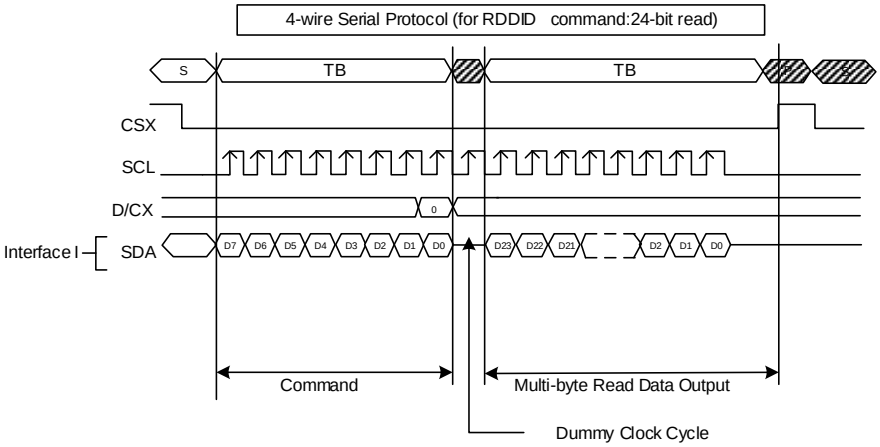
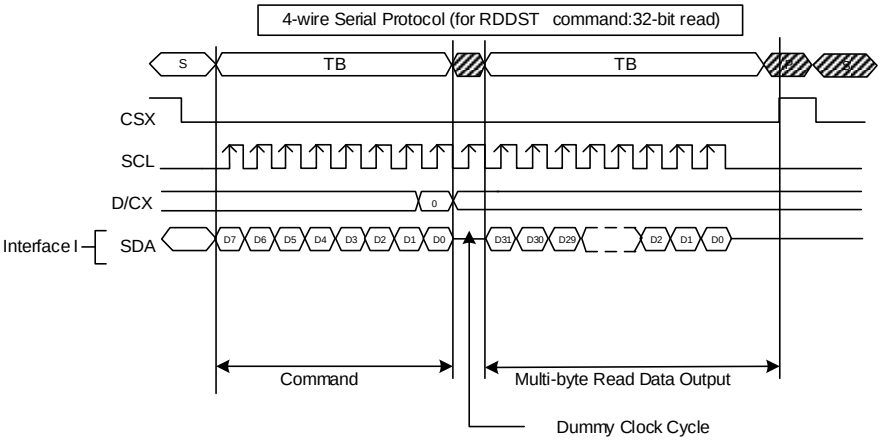


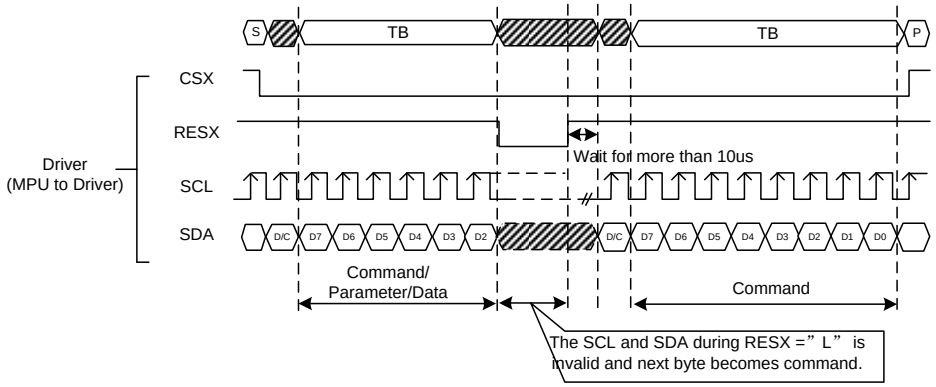
Figure 19.



3.1.8. Data Transfer Break and Recovery

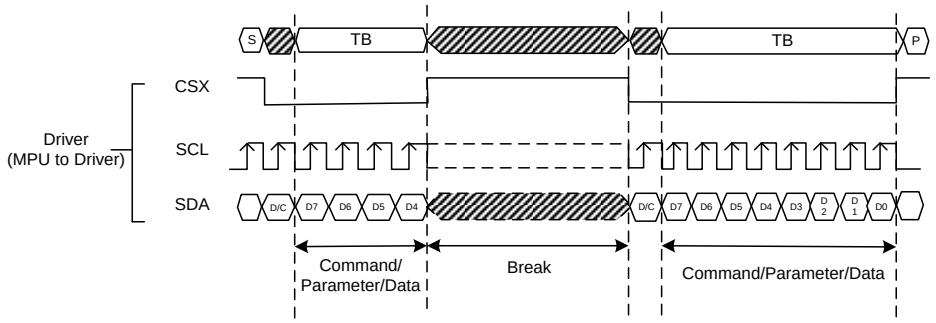
If there is a break in data transmission by RESX pulse, while transferring a command or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.

Figure 20.



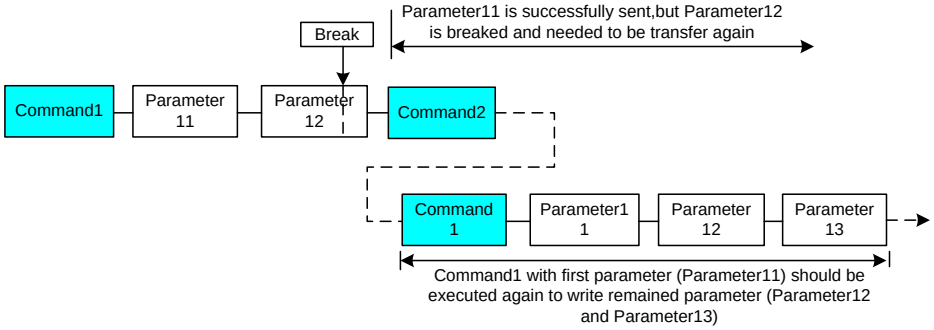
If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.

Figure 21.



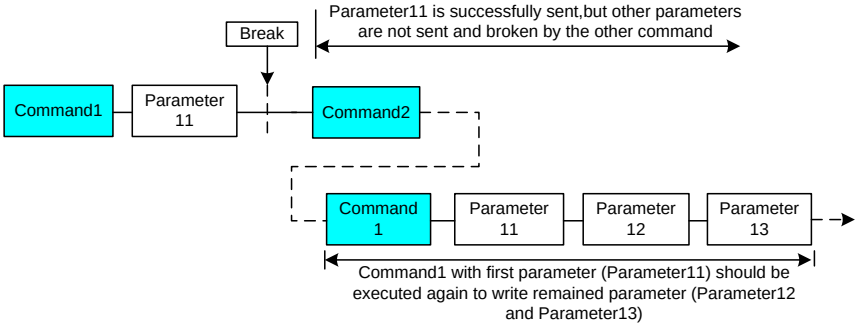
If two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

Figure 22.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.

Figure 23.



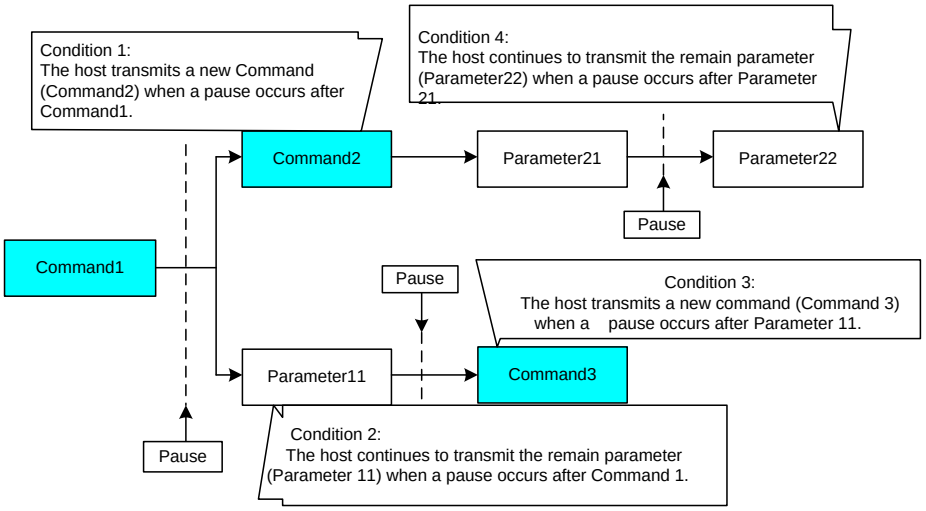
3.1.9. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then GC9B71 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters(if appropriate) or a new command when the chip select pin is next enabled as shown below.

This applies to the following 4 conditions:

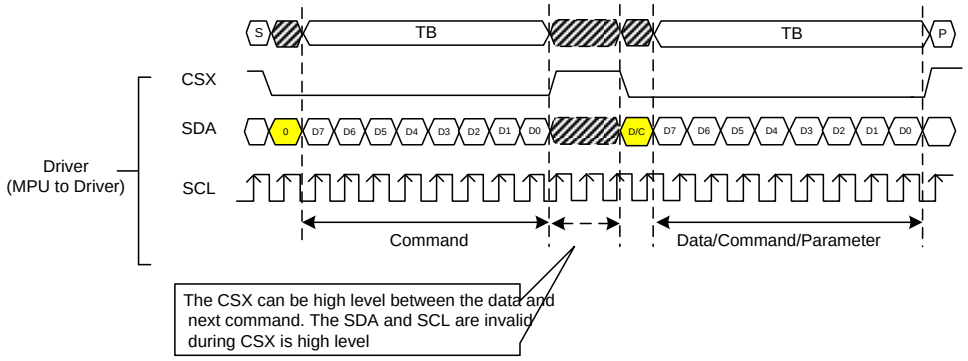
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

Figure 24.



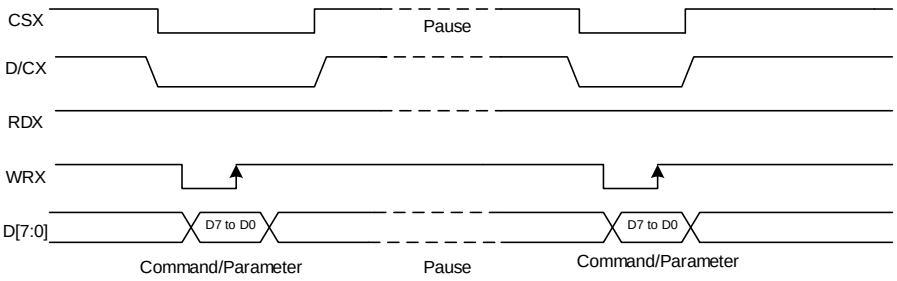
3.1.10. Serial Interface Pause (3_wire)

Figure 25.



3.1.11. Parallel Interface Pause

Figure 26.



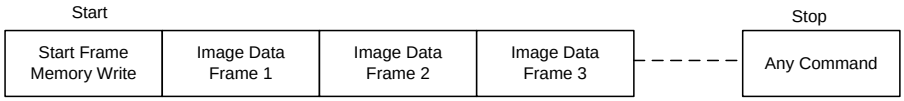
3.1.12. Data Transfer Mode

GC9B71 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

3.1.13. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.

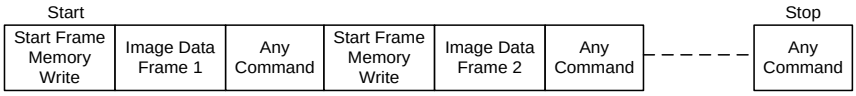
Figure 27.



3.1.14. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.

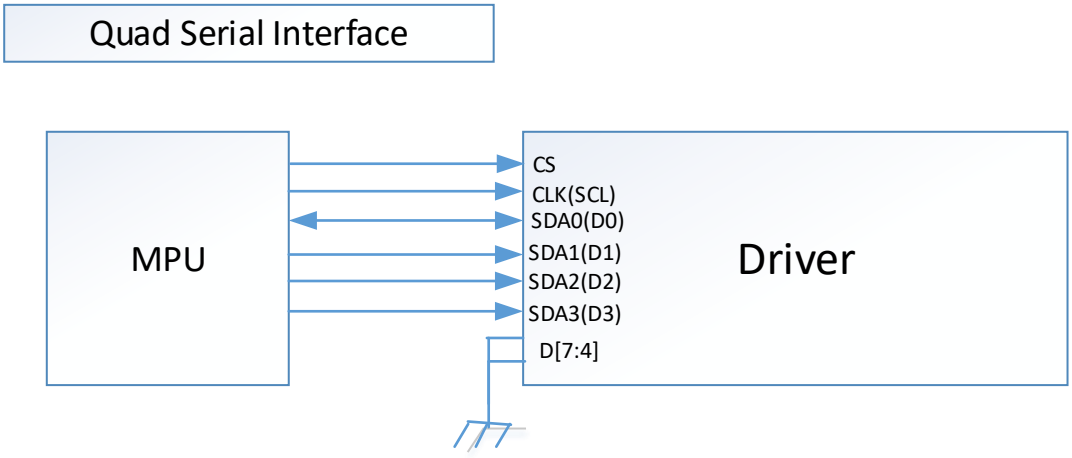
Figure 28.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.
Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

3.1.15. Quad Serial Peripheral Interface

The Quad Serial Peripheral Interface of GC9B71 can be selected by setting hardware pin IM [2:0] to “100”. The following shown figure is the example of interface with Quad Serial Peripheral Interface.

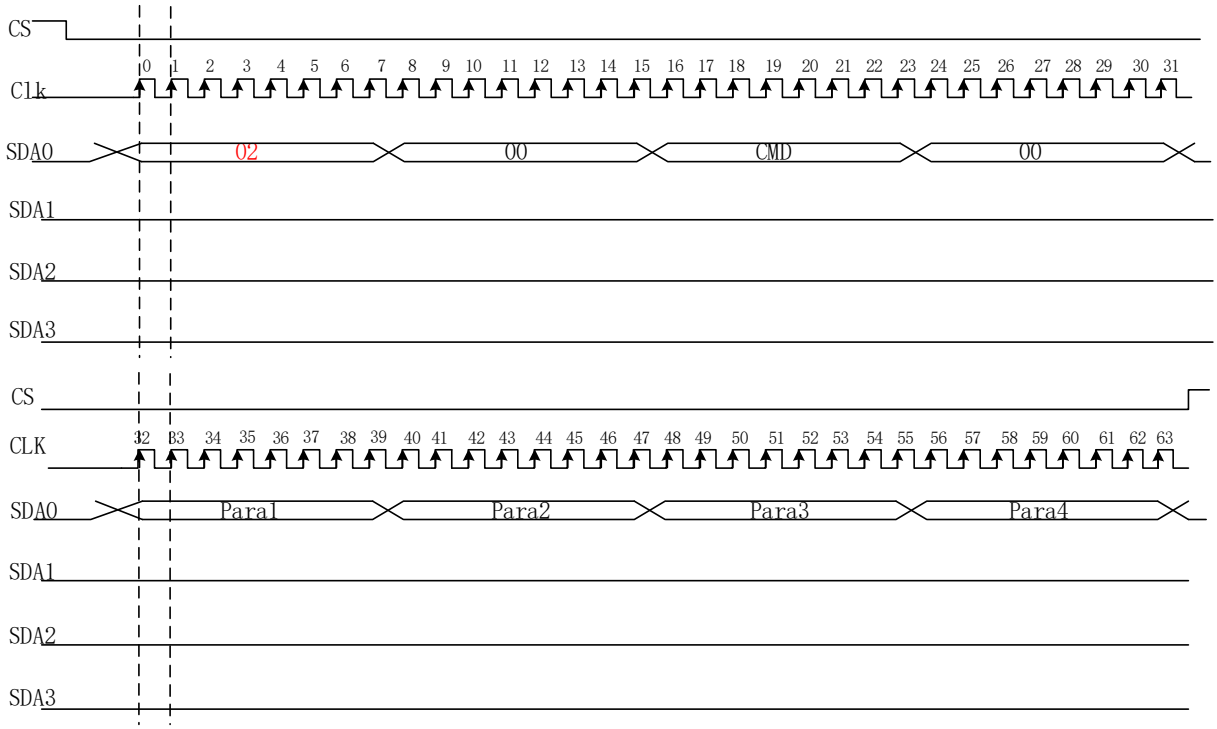


3.1.16. Write Cycle Sequence

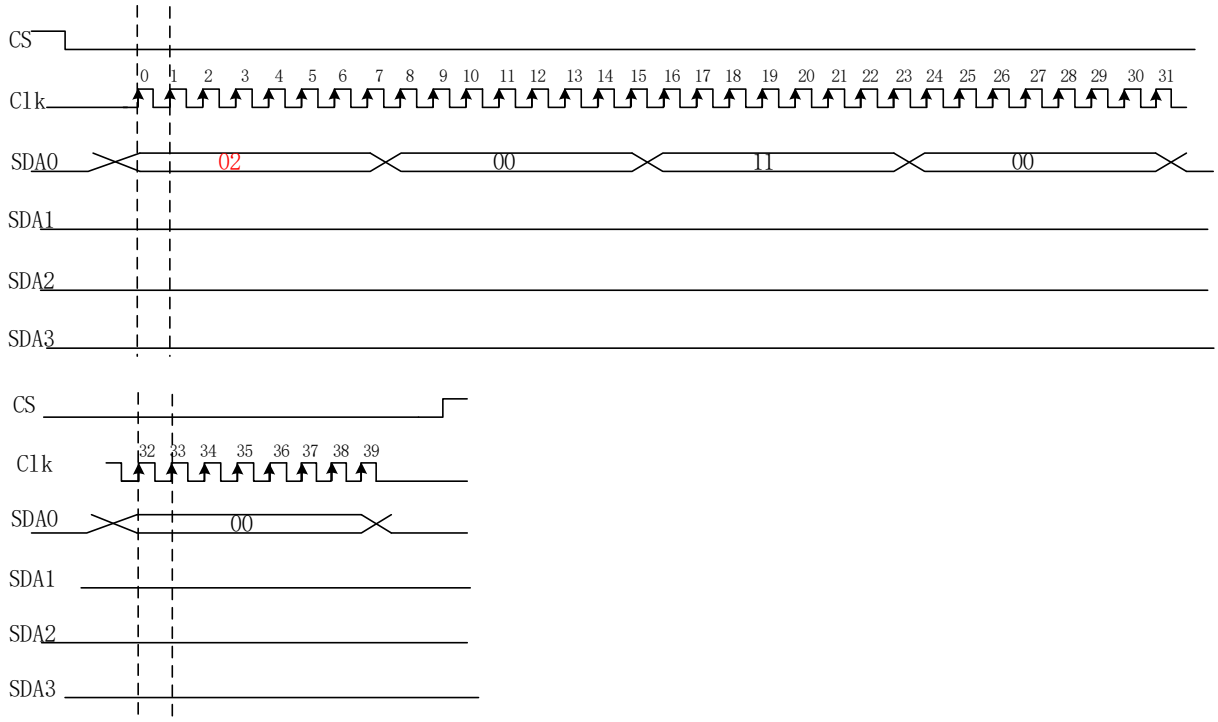
The GC9B71 reads the data at the rising edge of SCL signal.

The timing of Write Cycle Sequence is shown as below

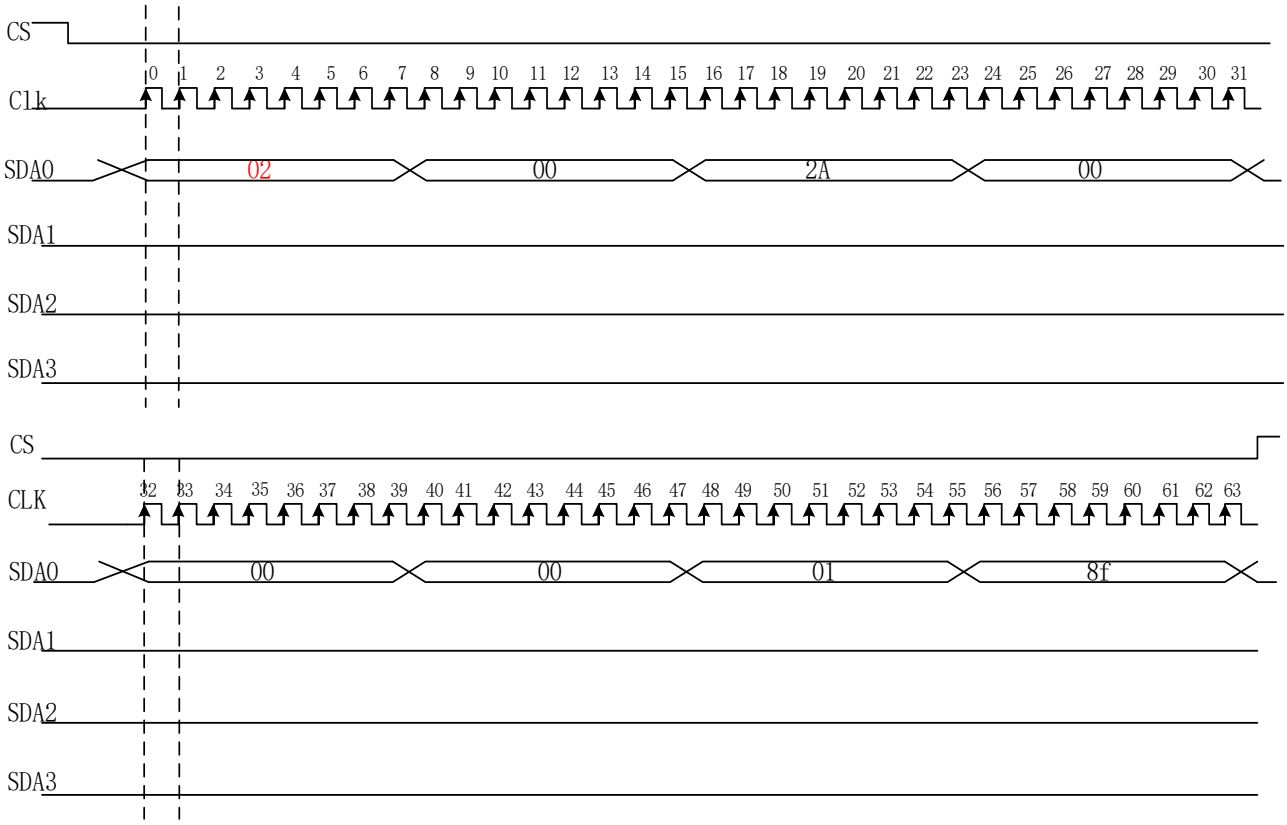
CMD_WR only use SDA0/D0, first byte=0x02



Eg:11



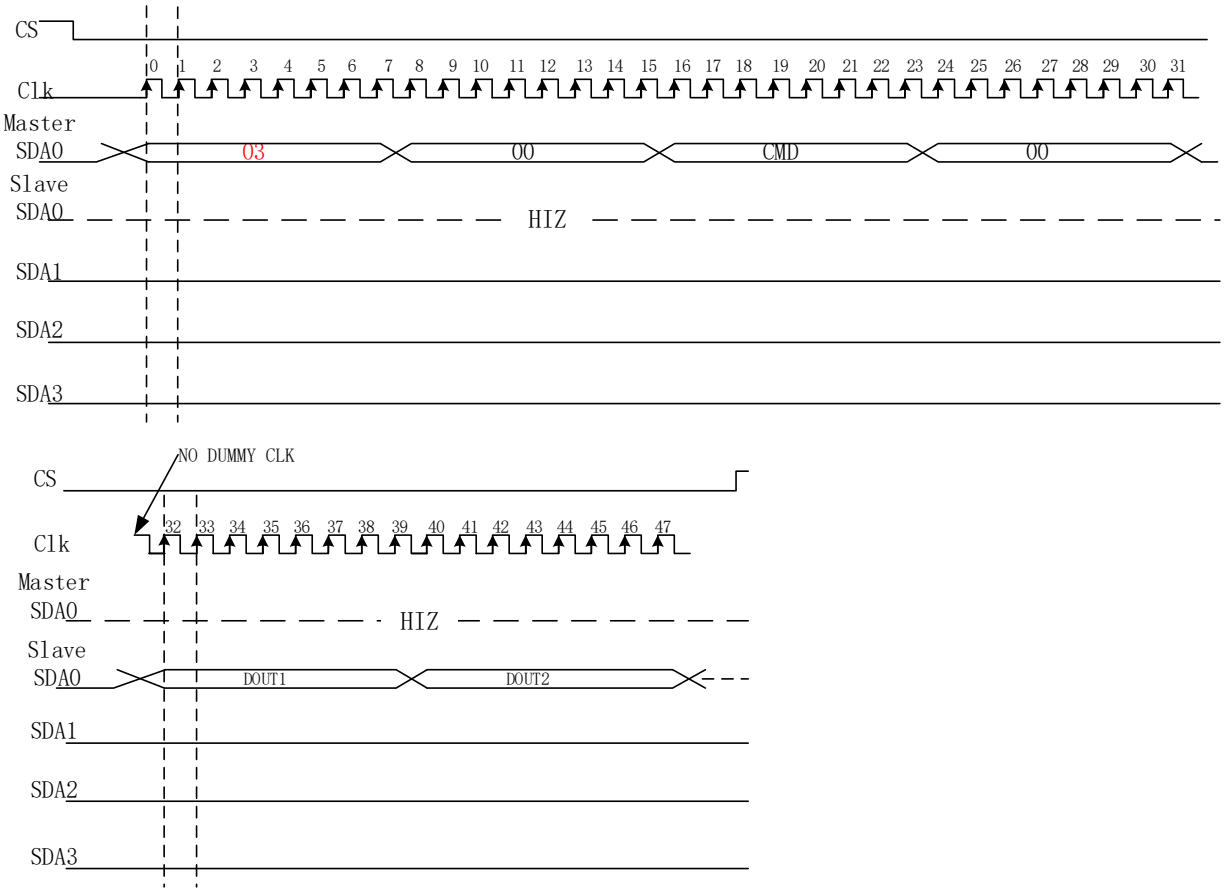
Eg:2A=00, 00, 01, 8f



3.1.17. Read Cycle Sequence

The timing of Read Cycle Sequence is shown as below

CMD_RD: Only Use SDA0/D0, First Byte=0x03



3.2. Display Data RAM (DDRAM)

GC9B71 has an integrated 360x360x18-bit graphic type static RAM. This 291,600 -bytes memory allows storing a 36xRGBx360 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.

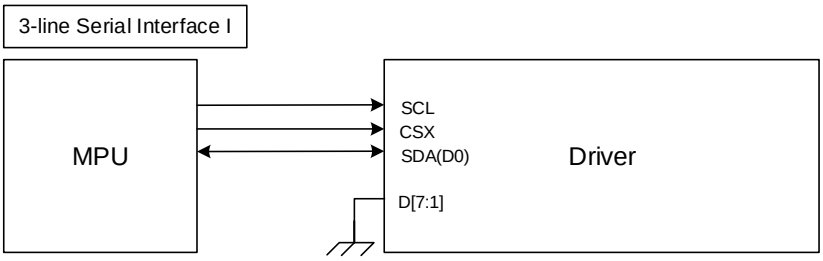
3.3. Display Data Format

GC9B71 supplies 8-bit parallel MCU interface with 8080-Ⅰ,3-/4-line serial interface ,The parallel MCU interface and serial interface mode can be selected by external pins IM [2:0]

3.3.1. 3-line Serial Interface

The 3-line/9-bit serial bus interface of GC9B71 can be used by setting external pin as IM [2:0] to “101” for serial interface. The shown figure is the example of 3-line SPI interface.

Figure39.



In 3-line serial interface, different display data format is available for three color depths supported by the LCM listed below.

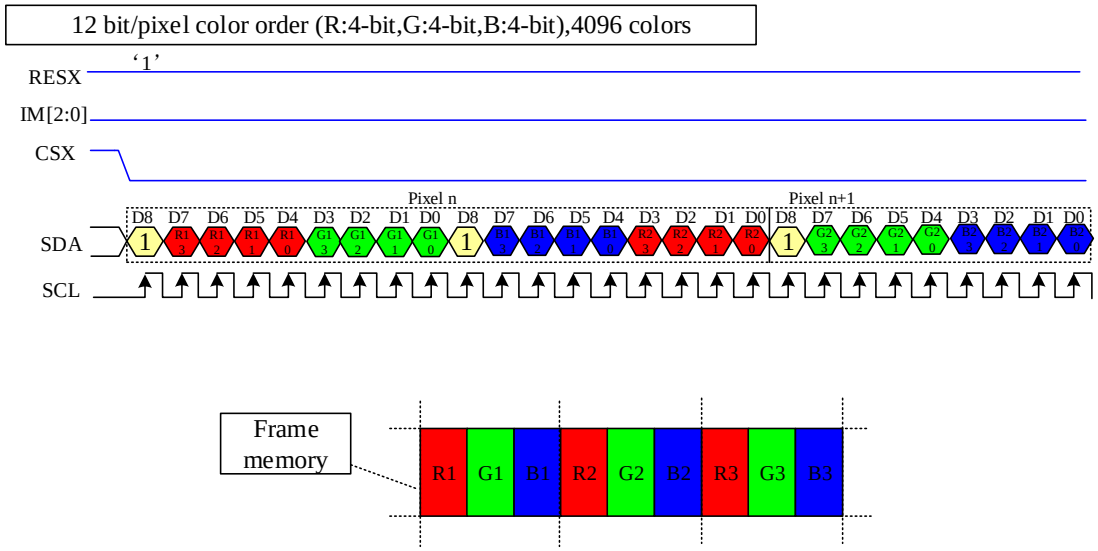
-4k colors, RGB 4, 4, 4 -bits input.

-65k colors, RGB 5, 6, 5 -bits input

-262k colors, RGB 6, 6, 6 -bits input.

1)4K-Colors:12-bit/pixel(RGB 4, 4, 4 -bits input).

Figure41.



Note 1: The pixel data with 12-bit color depth information.

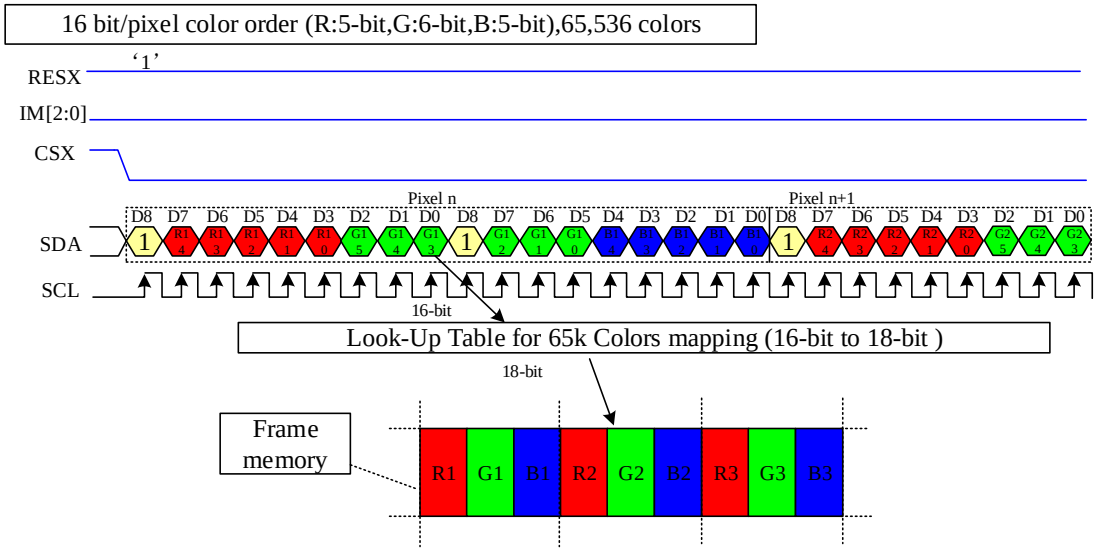
Note 2: The most significant bits are: Rx3, Gx3 and Bx3.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

2)65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

Figure41.



Note 1: The pixel data with 16-bit color depth information.

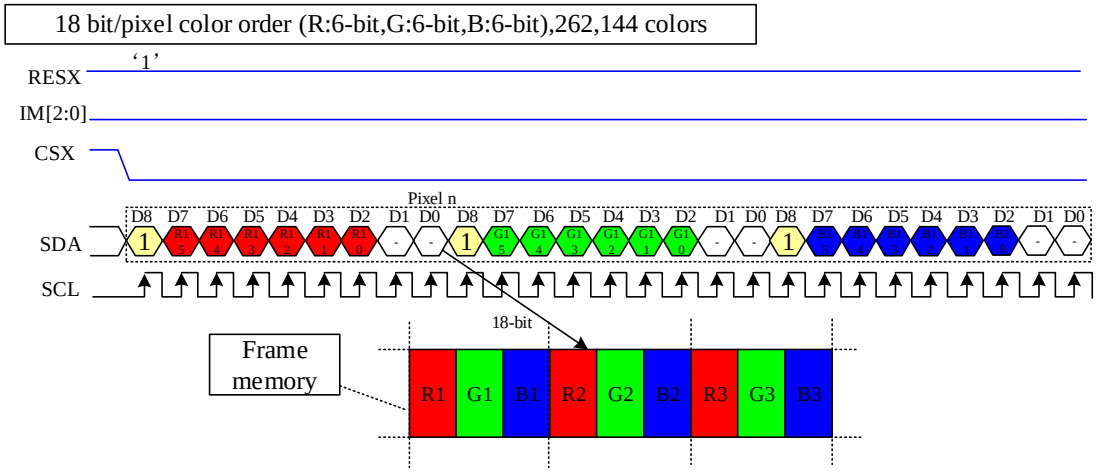
Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

3)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

Figure42.



Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

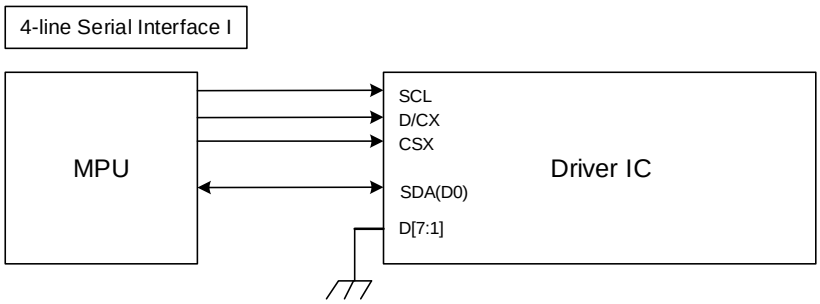
Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care - Can be set "0" or "1".

3.3.2. 4-line Serial Interface

The 4-line/8-bit serial bus interface of GC9B71 can be used by setting external pin as IM [2:0] to “111” for serial interface . The shown figure is the example of 4-line SPI interface.

Figure43.



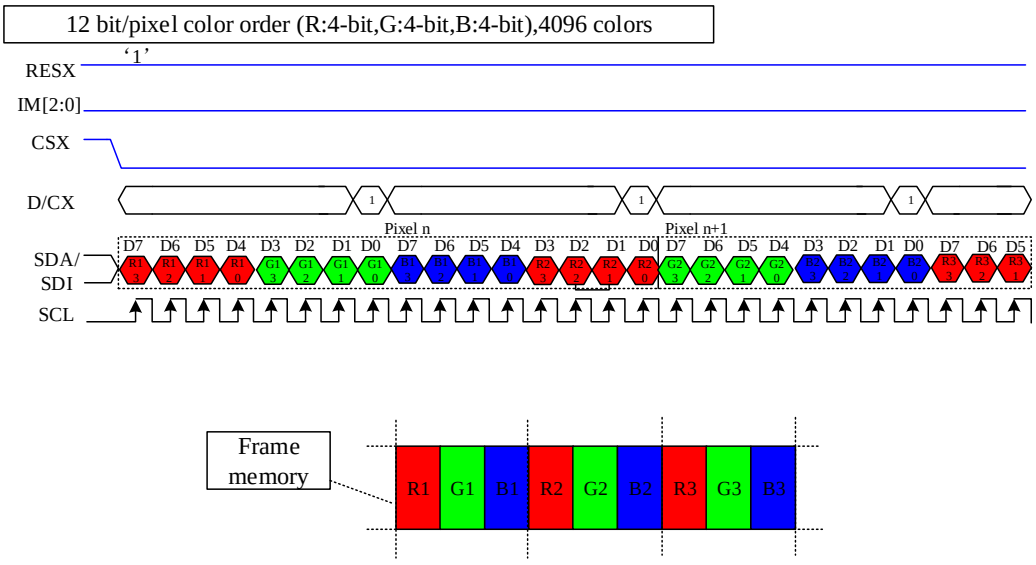
In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-4k colors, RGB 4, 4, 4 -bits input.

-65k colors, RGB 5, 6, 5 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.

Figure44.



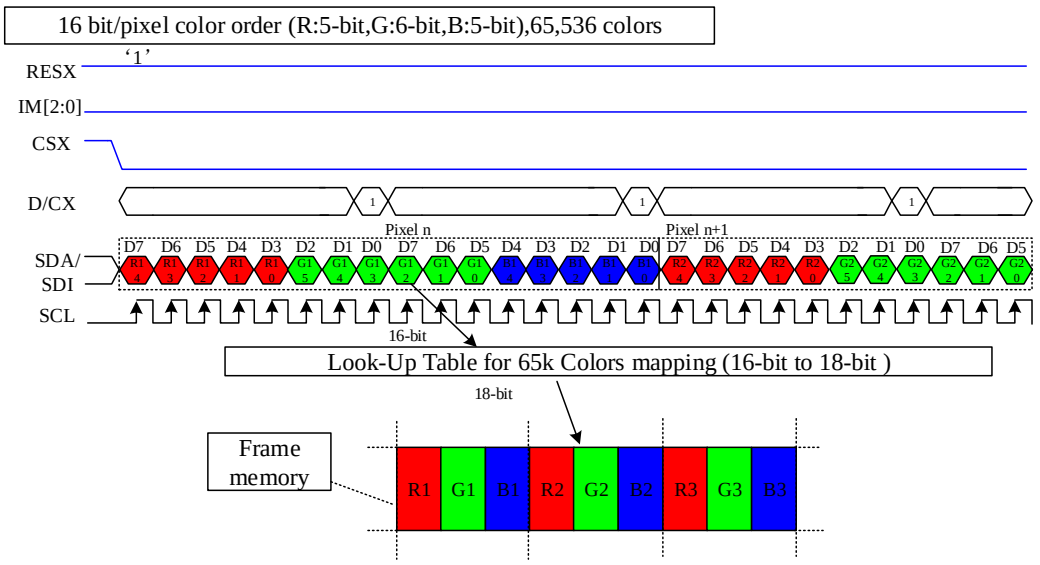
Note 1: The pixel data with 12-bit color depth information.

Note 2: The most significant bits are: Rx3, Gx3 and Bx3.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: ‘-‘= Don’t care –Can be set “0” or “1”.

Figure45.



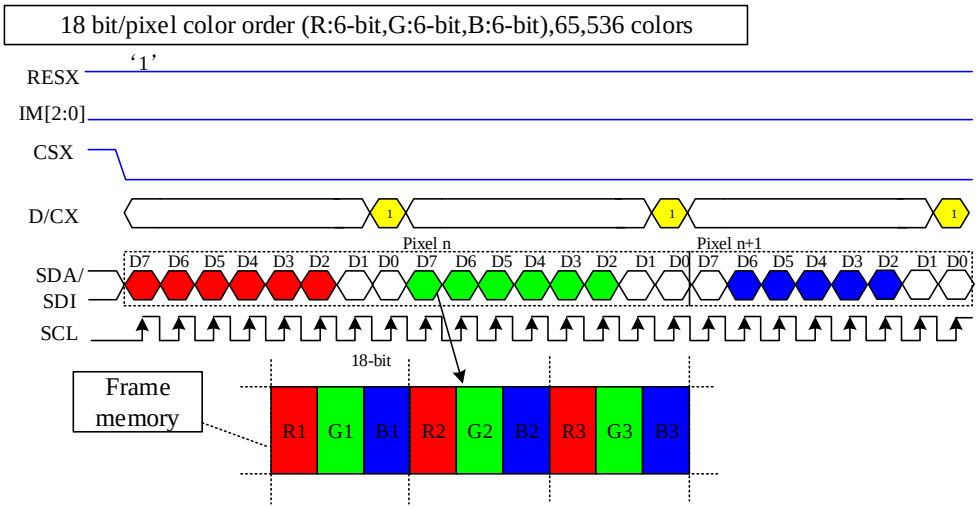
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

Figure46.



Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

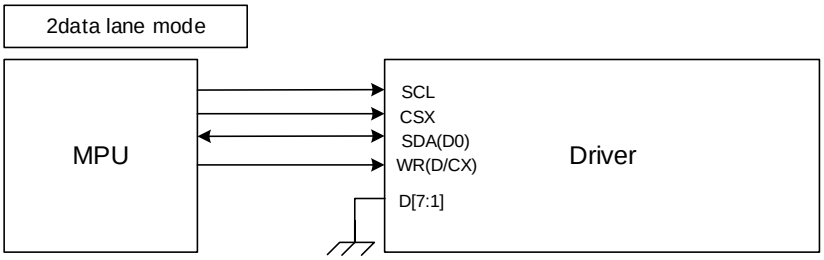
Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

3.3.3.2-data-lane mode

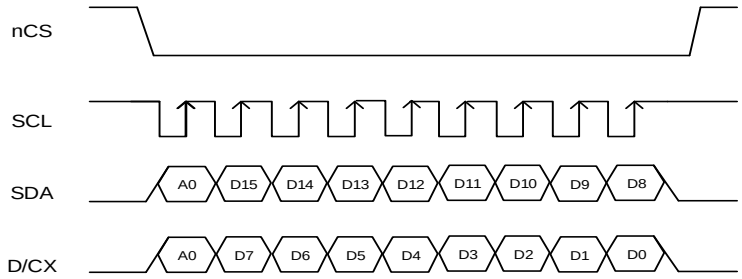
This mode is active when 2data_en (B1h[3]) set to “1” in 3-wire. Only frame pixel data write transitions are sent in 2-data-lane mode, register write/read is still sent in 3-wire.

The chip-select nCS (active low) enables and disables the serial interface. SCL is the serial data clock. SDA and DCX are serial data lines.The shown figure is the example of 3-line SPI interface.



Serial data must be input to SDA in the sequence A0, D15 to D10 and DCX in the sequence A0, D7 to D0. The GC9B71 reads the data at the rising edge of SCL signal. The first bit of serial data A0 is data/command flag. It must be set to "1", D15 to D0 bits are display RAM data.

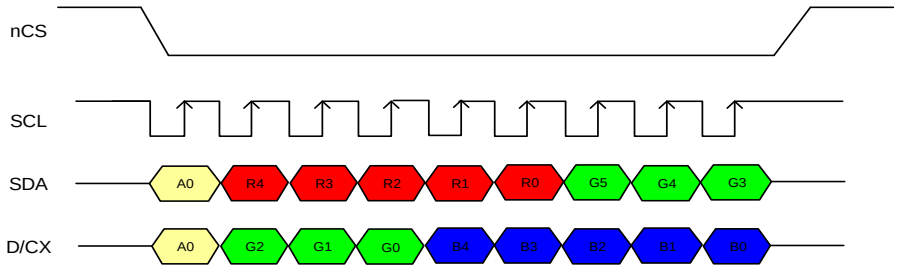
Figure47.



Five data formats are supported in 2-data-lane mode, which is indicated by 2data_mdt (B1h[2:0]) .

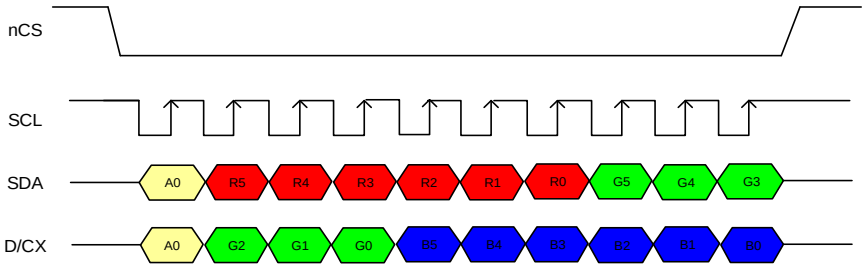
1)RGB565 1pixel/transition(65K color,2data_mdt[2:0]=’000’)

Figure48.



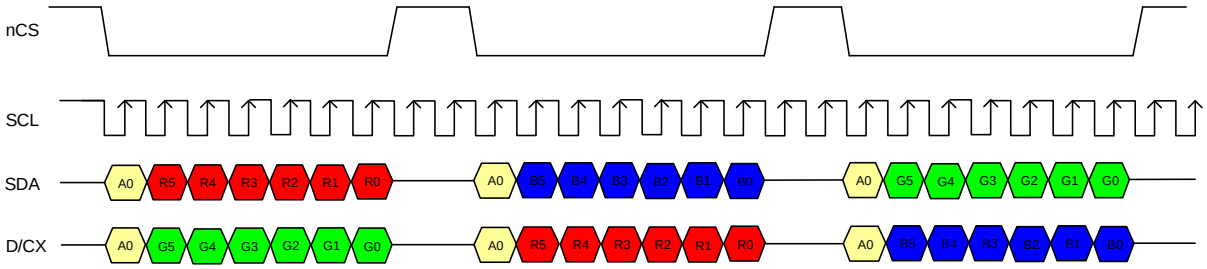
2)RGB666 1pixel/transition(262K color,2data_mdt[2:0]=’001’)

Figure49.



3)RGB666 2/3pixel/transition(262K color,2data_mdt[2:0]='010')

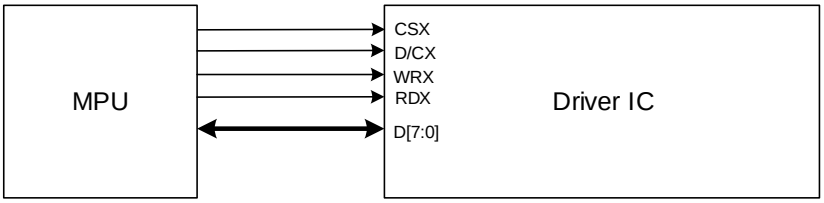
Figure50.



3.3.4. 8-bit Parallel MCU Interface

The 8080-Ⅰsystem 8-bit parallel bus interface of GC9B71 can be used by setting external pin as IM [2:0] to“000”.The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.

Figure53.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to “101”.

Table 11.

Count	0	1	2	3	4	…	717	718	719	720
D/CX	0	1	1	1	1	…	1	1	1	1
D7	C7	0R4	0G2	1R4	1G2	…	358R4	358G2	359R4	359G2
D6	C6	0R3	0G1	1R3	1G1	…	358R3	358G1	359R3	359G1
D5	C5	0R2	0G0	1R2	1G0	…	358R2	358G0	359R2	359G0
D4	C4	0R1	0B4	1R1	1B4	…	358R1	358B4	359R1	359B4
D3	C3	0R0	0B3	1R0	1B3	…	358R0	358B3	359R0	359B3
D2	C2	0G5	0B2	1G5	1B2	…	357G5	358B2	358G5	359B2
D1	C1	0G4	0B1	1G4	1B1	…	357G4	358B1	358G4	359B1
D0	C0	0G3	0B0	1G3	1B0	…	357G3	358B0	358G3	359B0

2) 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Table12.

Count	0	1	2	3	…	1078	1079	1080
D/CX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	359R5	359G5	359B5
D6	C6	0R4	0G4	0B4	…	359R4	359G4	359B4
D5	C5	0R3	0G3	0B3	…	359R3	359G3	359B3
D4	C4	0R2	0G2	0B2	…	359R2	359G2	359B2
D3	C3	0R1	0G1	0B1	…	359R1	359G1	359B1
D2	C2	0R0	0G0	0B0	…	359R0	359G0	359B0
D1	C1				…			
D0	C0				…			

3.3.5. Quad Serial Peripheral Interface

In quad serial Peripheral interface, different display data format is available for three color depths supported by the LCM listed below.

-16.7M colors RGB 8, 8, 8-bits input with dither on by setting DBI[2:0]=7(3Ah) and DTR_EN=1 (B1h)

-262k colors, RGB 6, 6, 6 -bits input.

-65k colors, RGB 5, 6, 5 -bits input

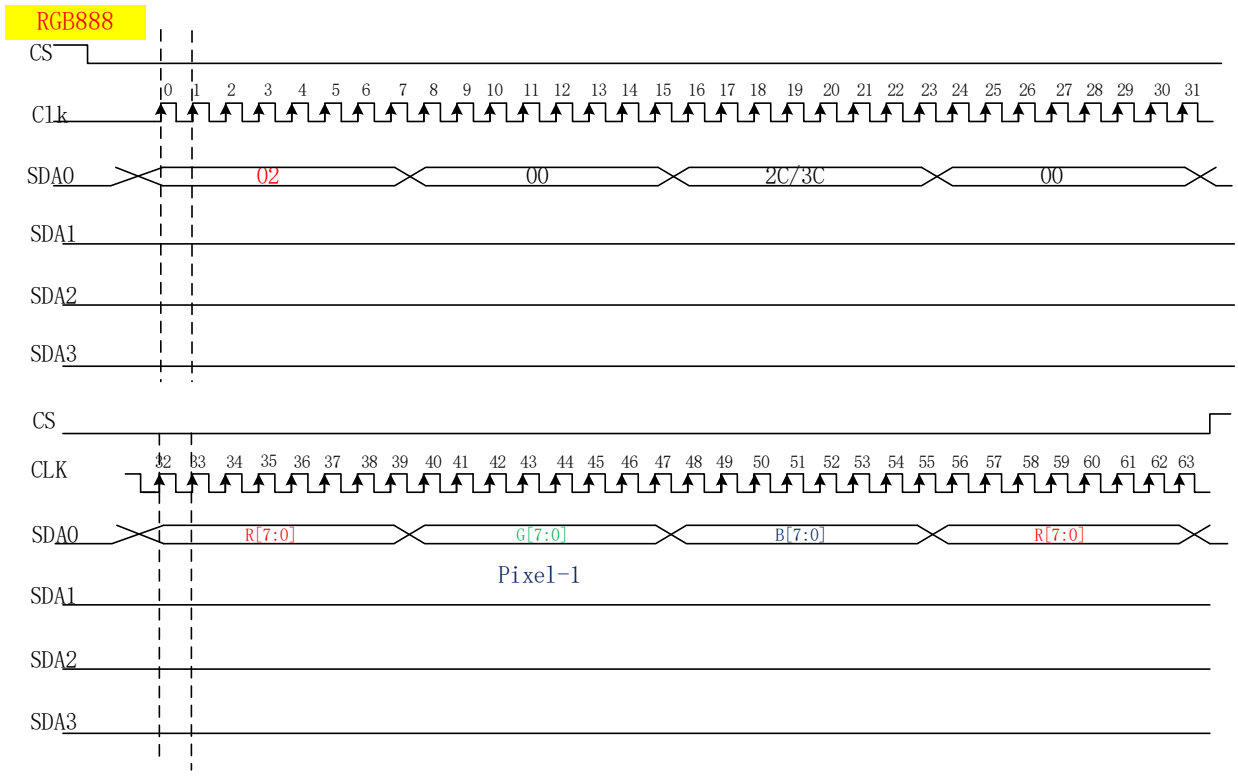
-256 colors, RGB 3, 3, 2 -bits input

-8 colors，RGB 1, 1, 1-bits input

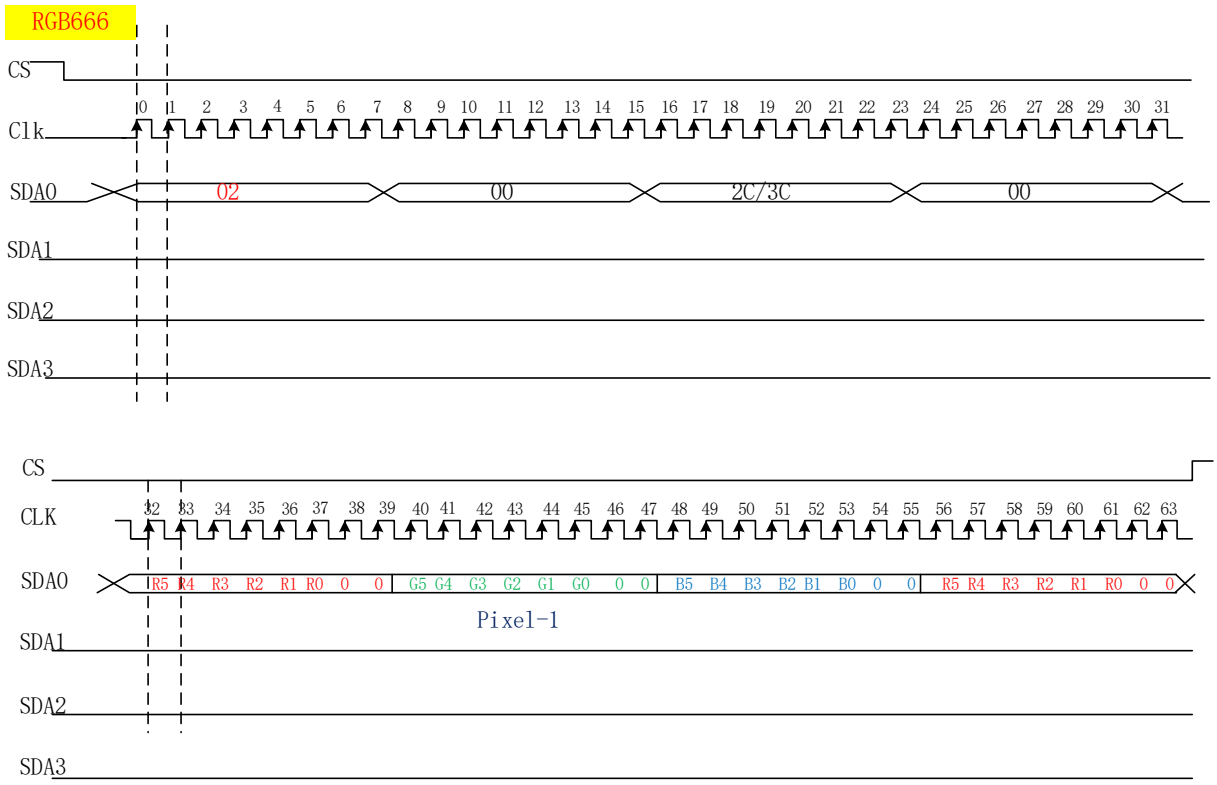
-256 gray，data：BIN00000000~BIN11111111

1wire data: only use SDA0/D0, first byte=0x02

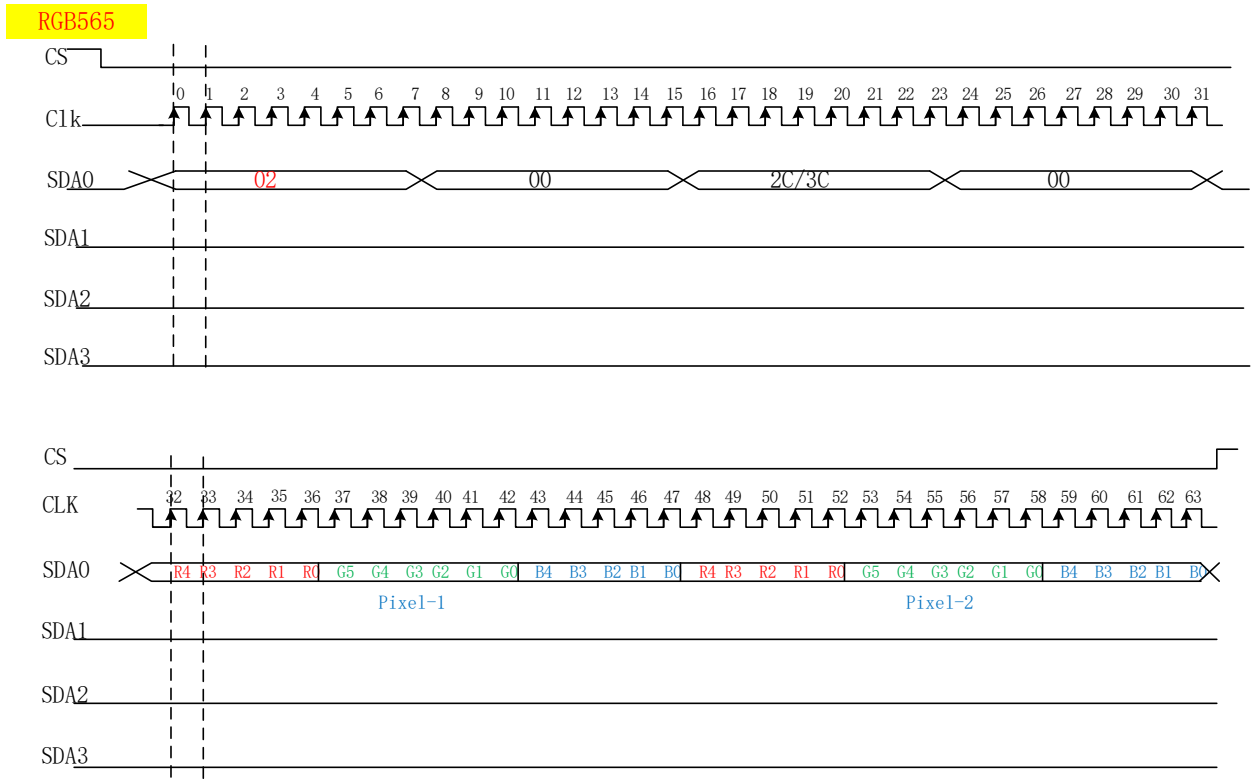
1） 16.7M-Colors:24-bit/pixel (RGB 8, 8, 8 -bits input).



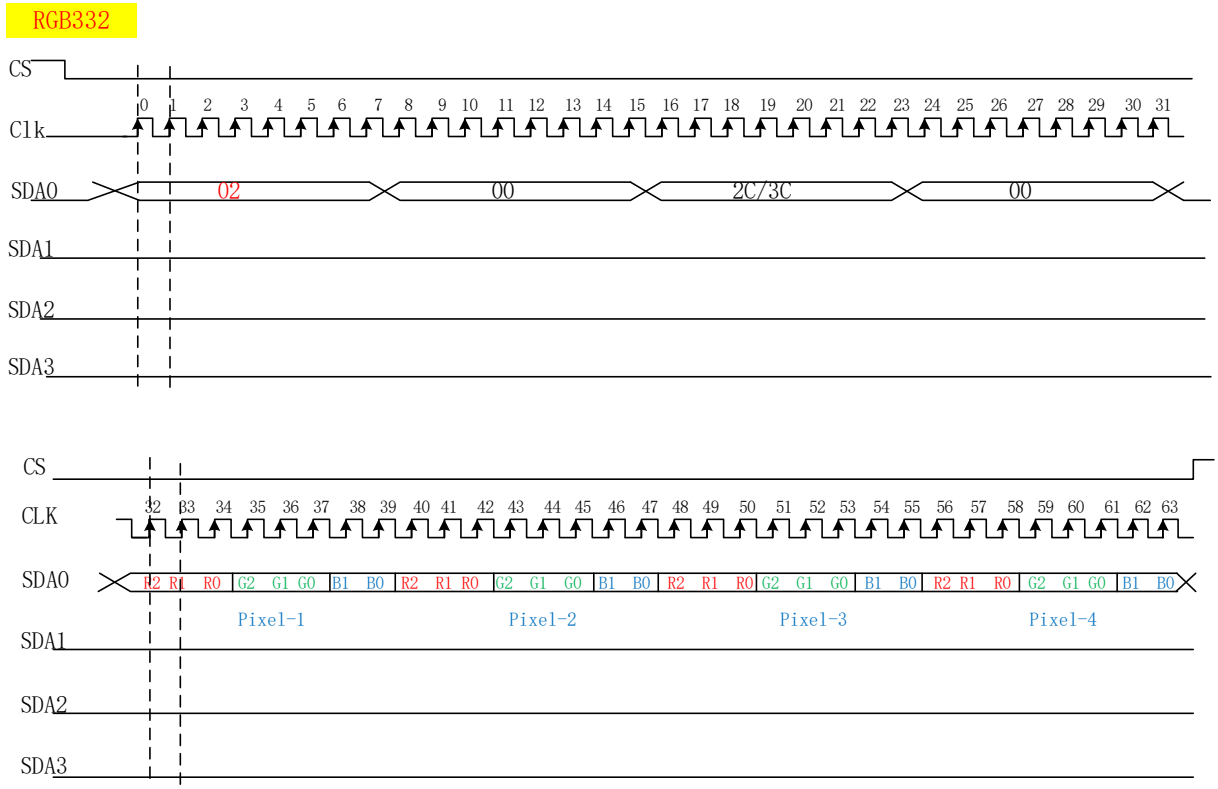
2） 262k-Colors:18-bit/pixel (RGB 6, 6, 6-bits input).



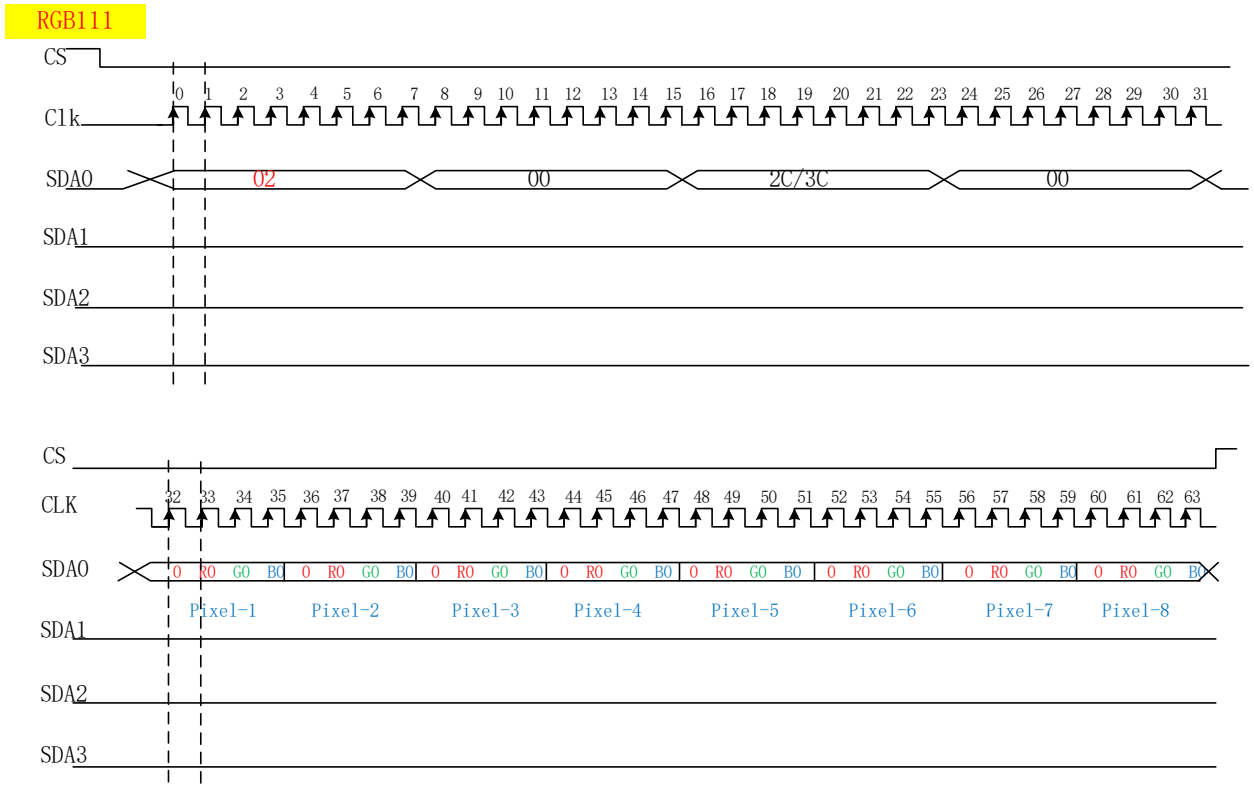
3） 65k-Colors:16-bit/pixel (RGB 5, 6,5 -bits input).



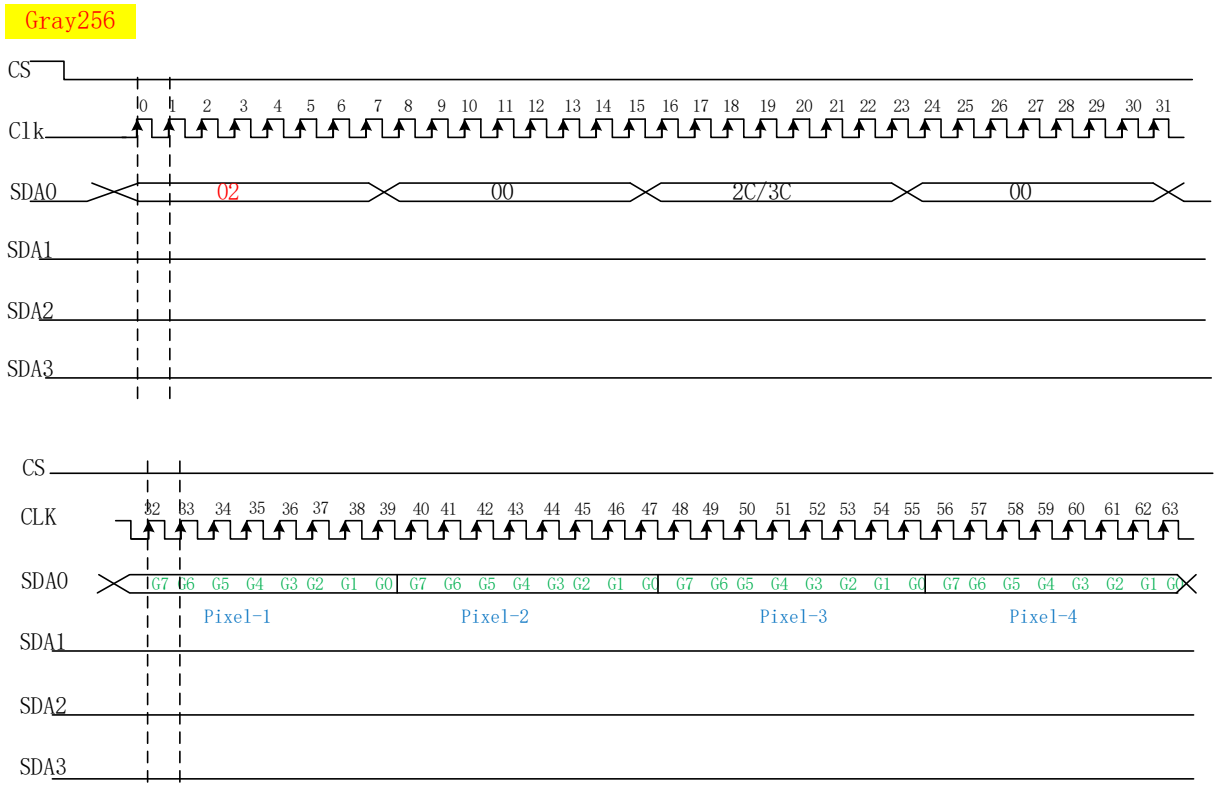
4） 256-Colors:8-bit/pixel (RGB 3, 3, 2 -bits input).



5） **8-Colors:3-bit/pixel (RGB 1, 1, 1 -bits input).**

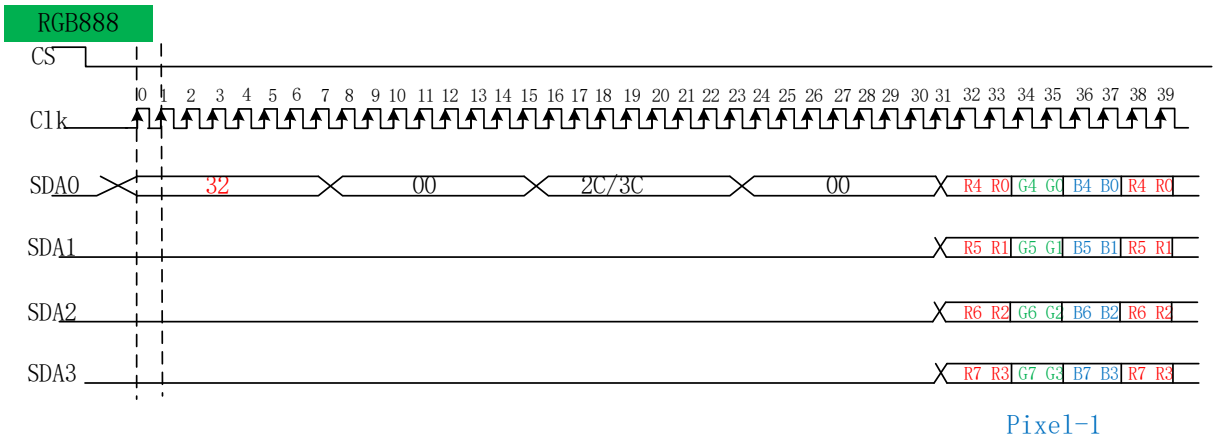


6） **256gray (data：bin0~bin11111111).**

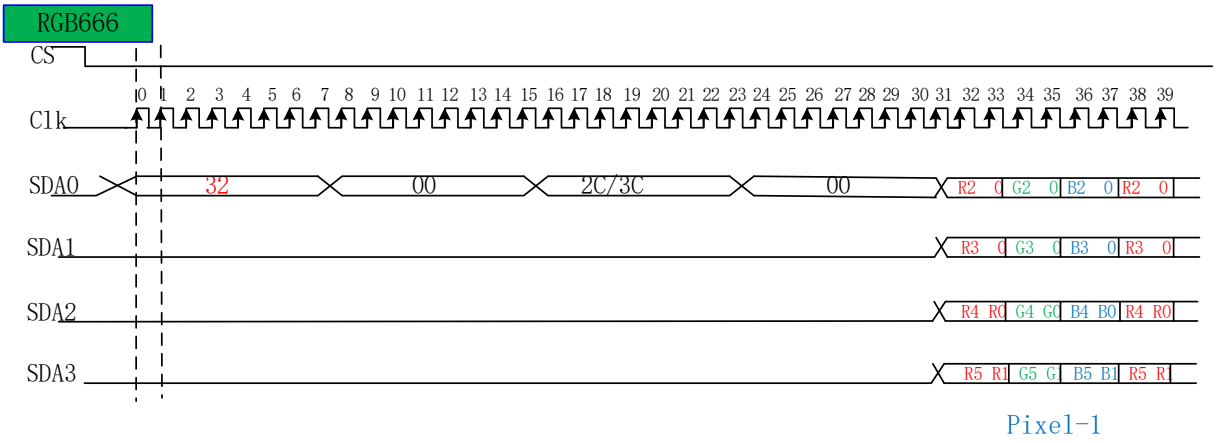


4wire data 1wire Addr: first byte=0x32

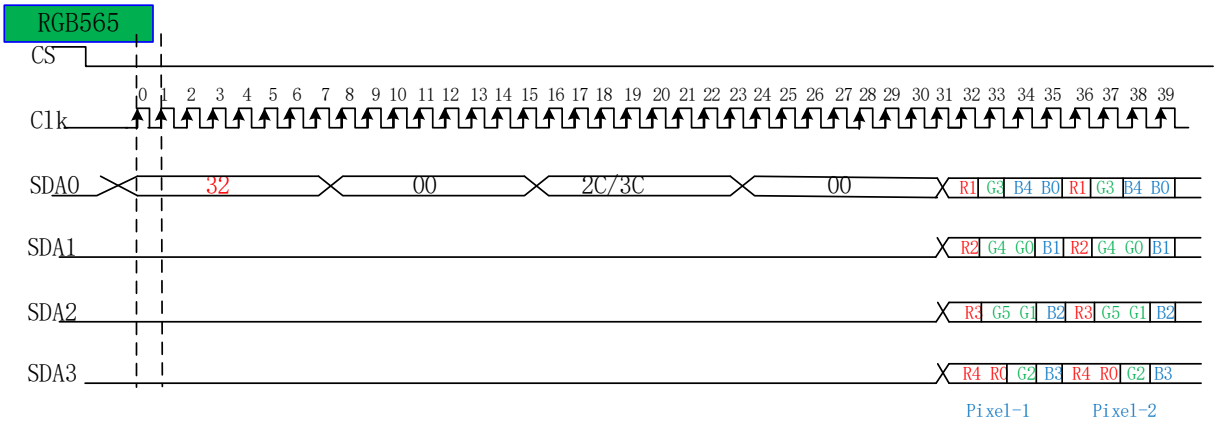
1） 16.7M-Colors:24-bit/pixel (RGB 8, 8, 8 -bits input).



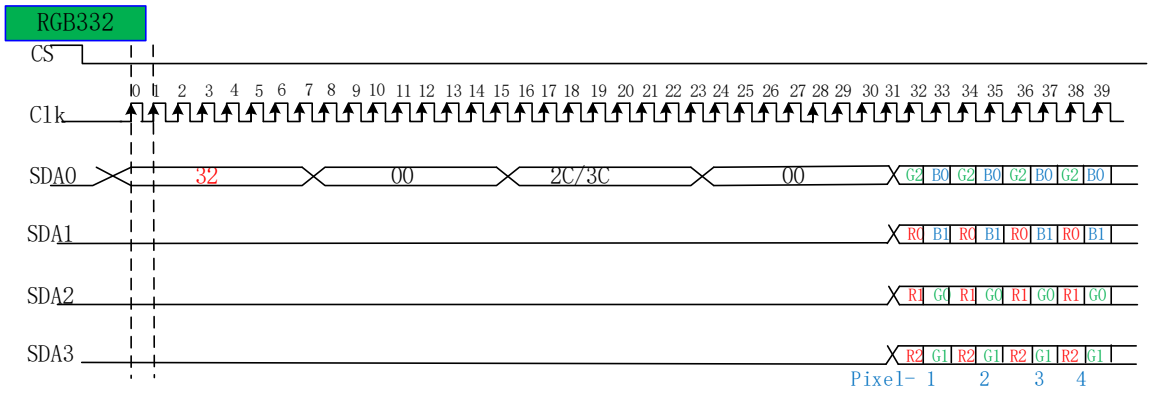
2） 262k-Colors:18-bit/pixel (RGB 6, 6, 6 -bits input).



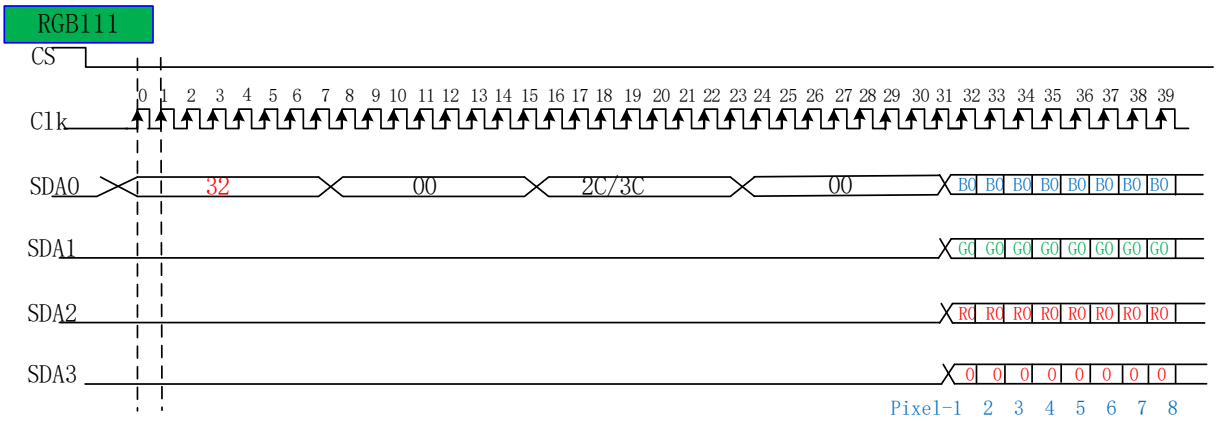
3） 65k-Colors:16-bit/pixel (RGB 5, 6,5 -bits input).



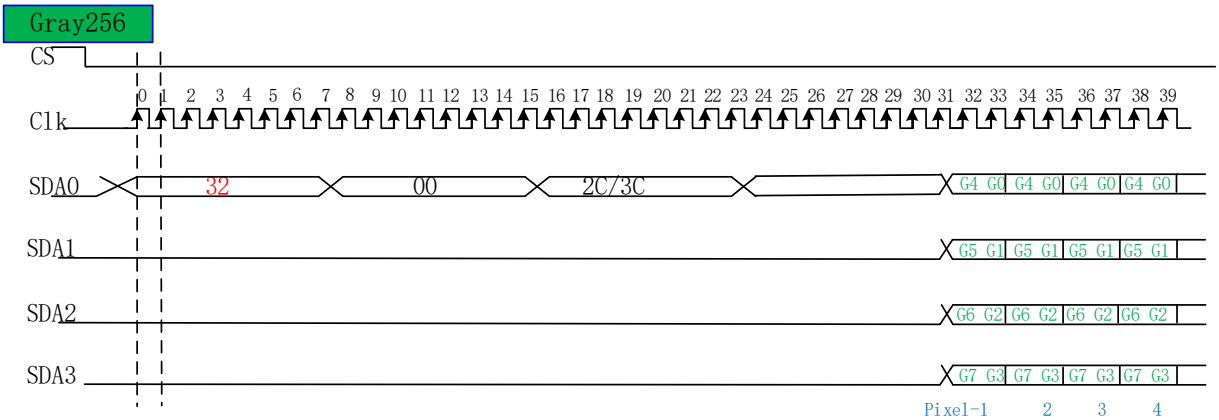
4） 256-Colors:8-bit/pixel (RGB 3, 3, 2 -bits input).



5） 8-Colors:3-bit/pixel (RGB 1, 1, 1 -bits input).

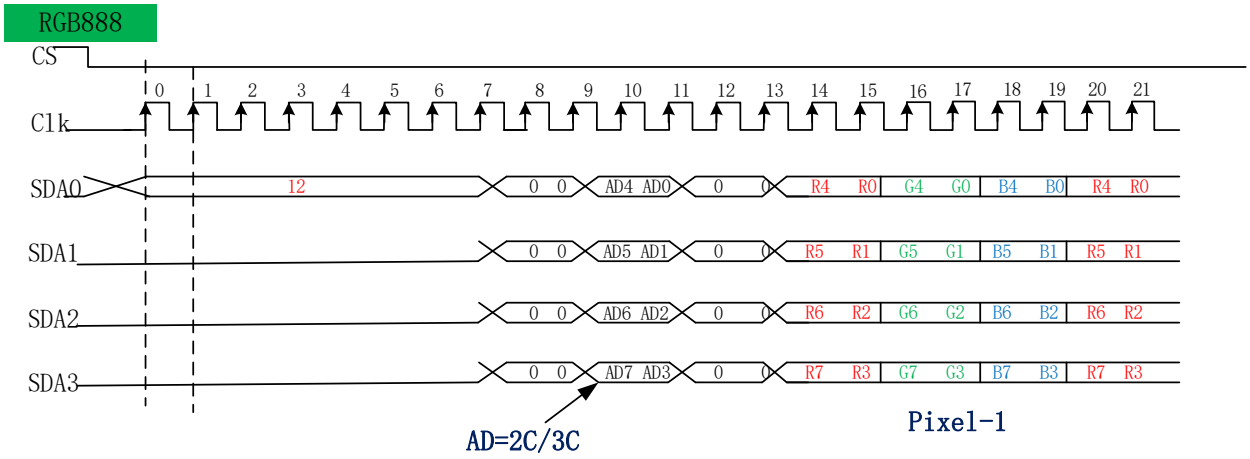


6） 256gray (data：bin0~bin11111111).

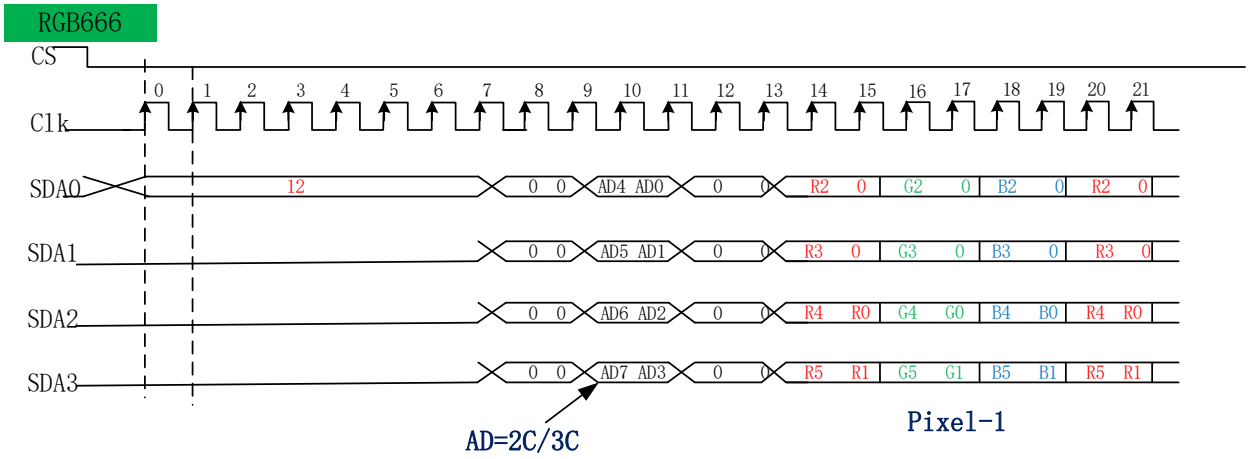


4wire data 4wire Addr: first byte=0x12

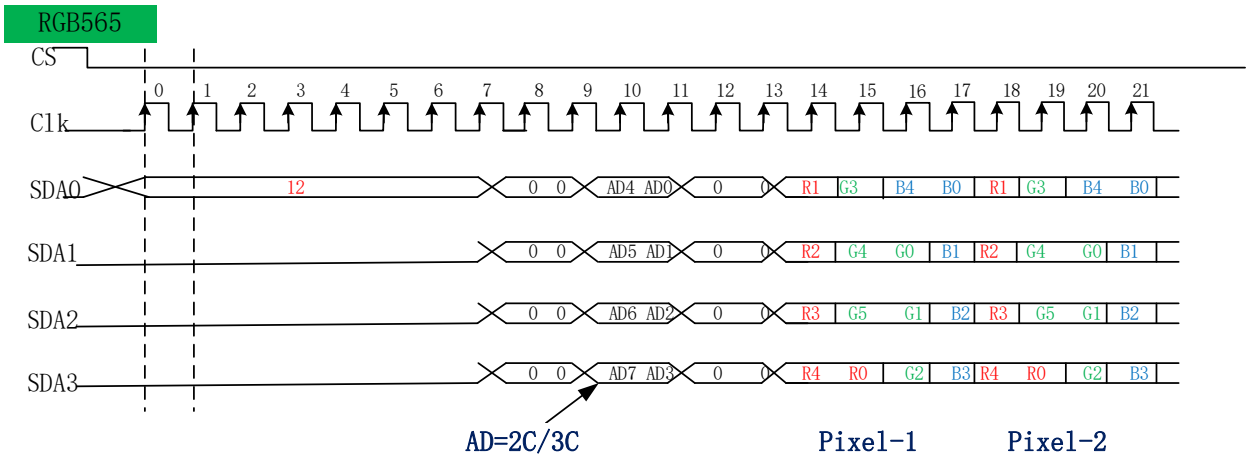
1）16.7M-Colors:24-bit/pixel (RGB 8, 8, 8 -bits input).



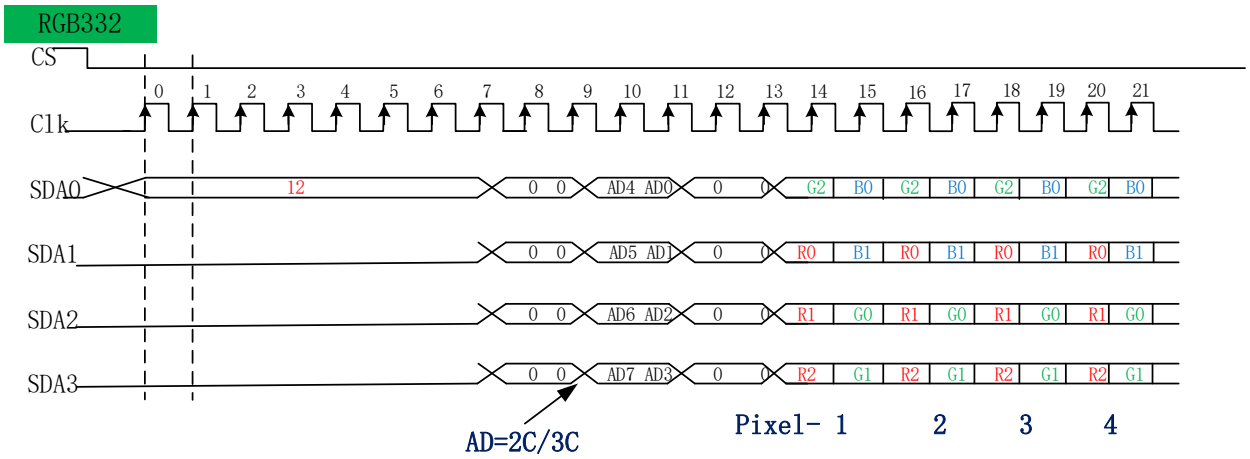
2）262k-Colors:18-bit/pixel (RGB 6, 6, 6-bits input).



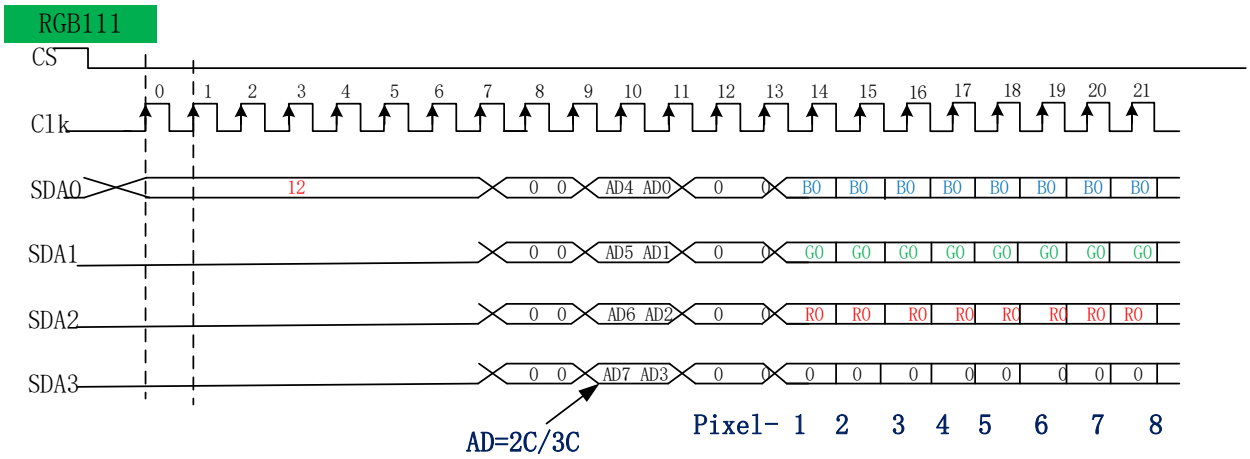
3）65k-Colors:16-bit/pixel (RGB 5, 6,5 -bits input).



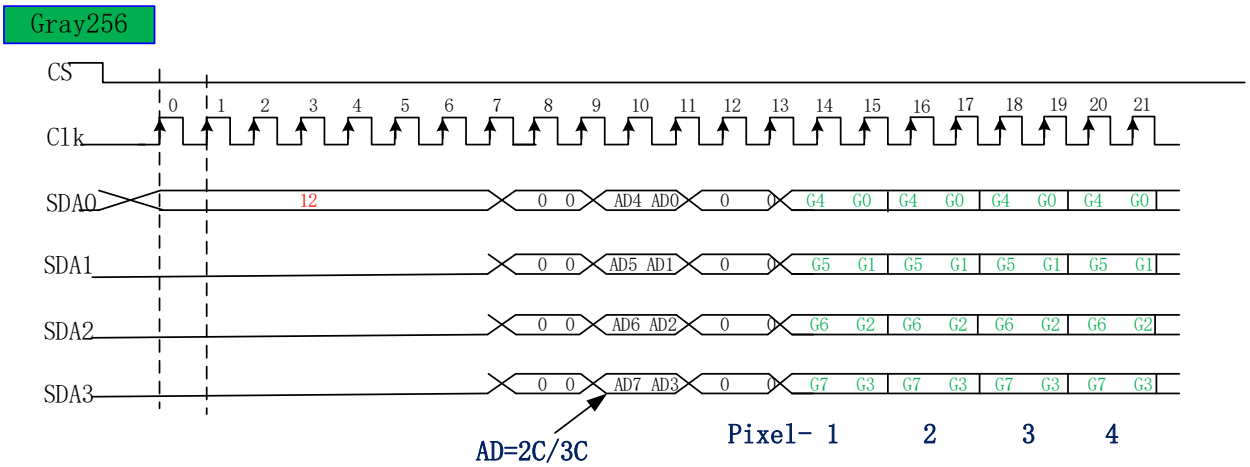
4）256-Colors:8-bit/pixel (RGB 3, 3, 2 -bits input).



5）8-Colors:3-bit/pixel (RGB 1, 1, 1 -bits input).



6）256gray (data：bin0~bin11111111).

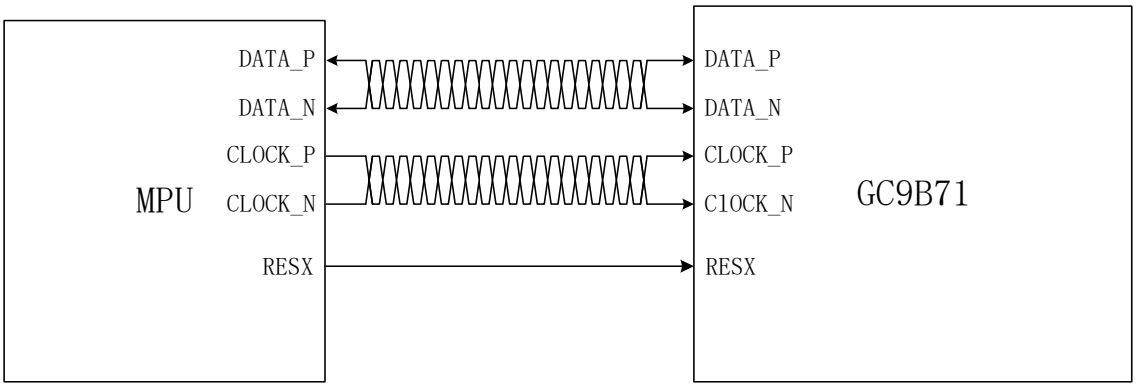


3.4. MIPI (Mobile Industry Processor Interface)

GC9B71supports MIPI DSI which can be enabled or disabled by external IM [2:0] pin. GC9B71can be accessed through one PHY lane module which communicates via two lines to a complementary part at the other side of the lane interconnects. The communication can be separated two different levels between the MCU and GC9B71:

- Low level communication what is done on the interface level.
- High level communication what is done on the packet level.

GC9B71 uses data and clock lane differential pairs for DSI, The data lane (D0P and D0N) is used for data communication and clock lane (DKP and DKN) is used to transmit the clock signal. The Mobile Industry Processor Interface (MIPI) can be used for communication between the processor and DSI-compliant LCD driver chip. The selection of this interface is done when IM [2:0] =110.



Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode. High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to GC9B71 and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane pair state code	Line DC Voltage Levels		High Speed	Low Power	
	D0_P	D0_N	Burst mode	DK_P	DK_N
HS-0	Low(HS)	High(HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low(LP)	Low(LP)	Not define	Bridge	Space
LP-01	Low(LP)	High(LP)	Not define	HS-Request	Mark-0
LP-10	High(LP)	Low(LP)	Not define	LP-Request	Mark-1
LP-11	High(LP)	High(LP)	Not define	Stop	Note 2

Notes: (1) Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair

is in the High Speed (HS) mode.

(2) If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

3.4.1. Interface Level Communication – Clock Lanes

DK_P/N lanes can be driven into three different power modes:

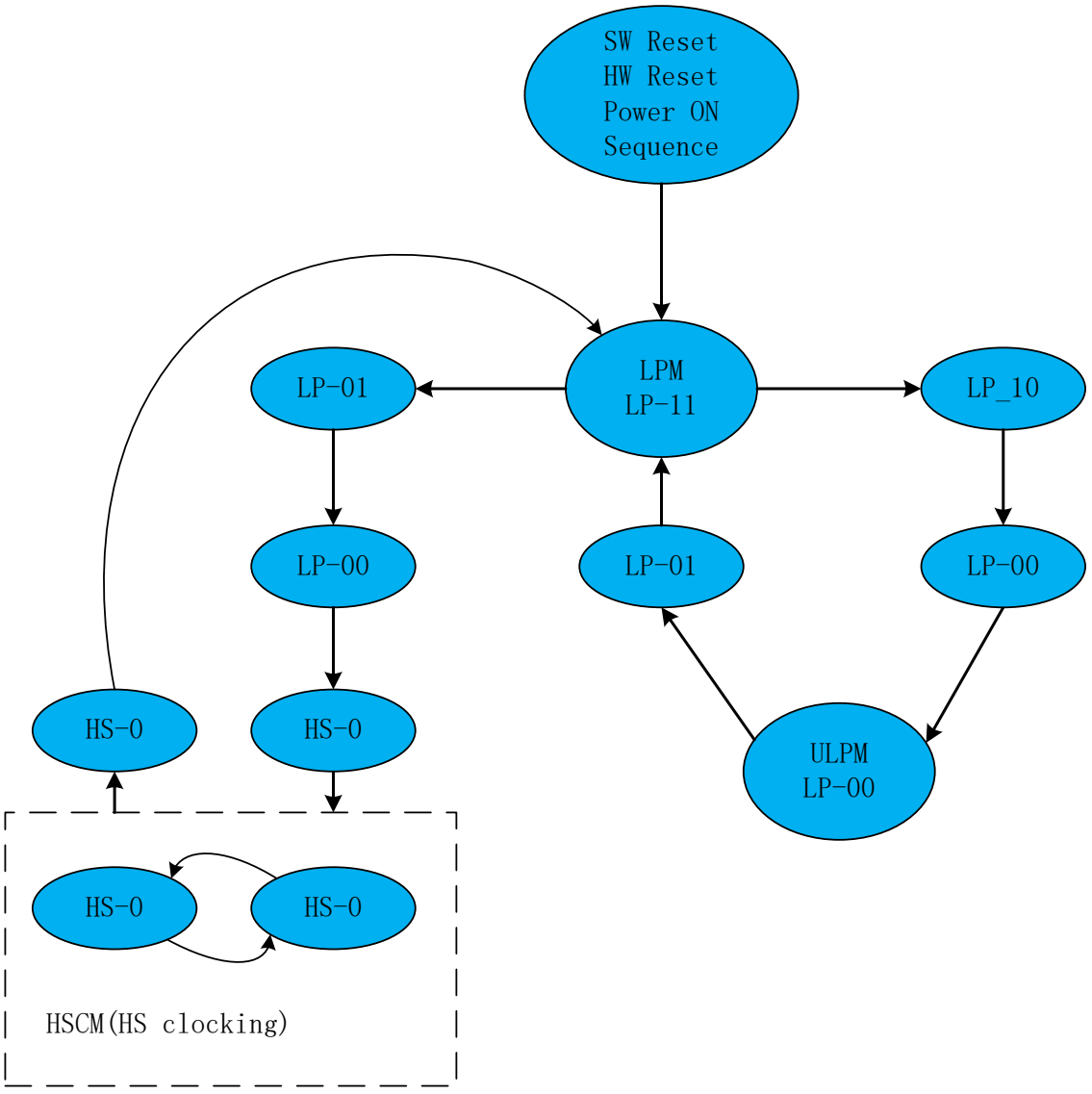
- Low Power Mode (LPM)
- Ultra Low Power Mode (ULPM)
- High Speed Clock Mode (HSCM)

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

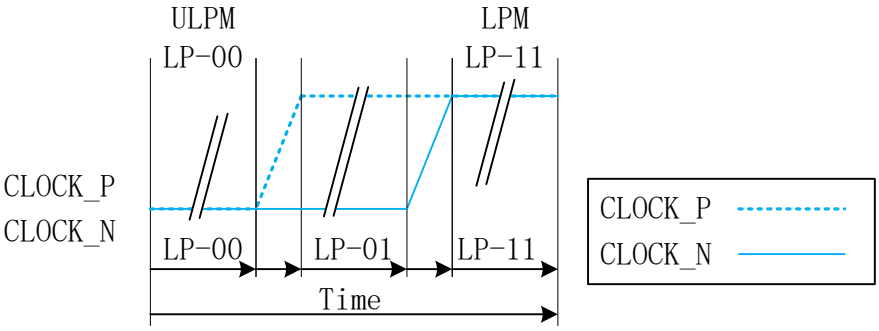


3.4.1.1. Low Power Mode (LPM)

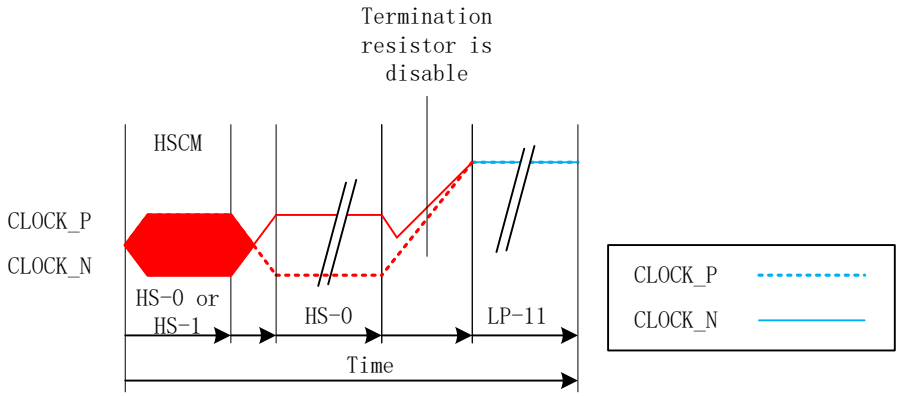
DK_P/N lanes can be driven to the Low Power Mode (LPM), when DK lanes are entering LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence =>LP-11

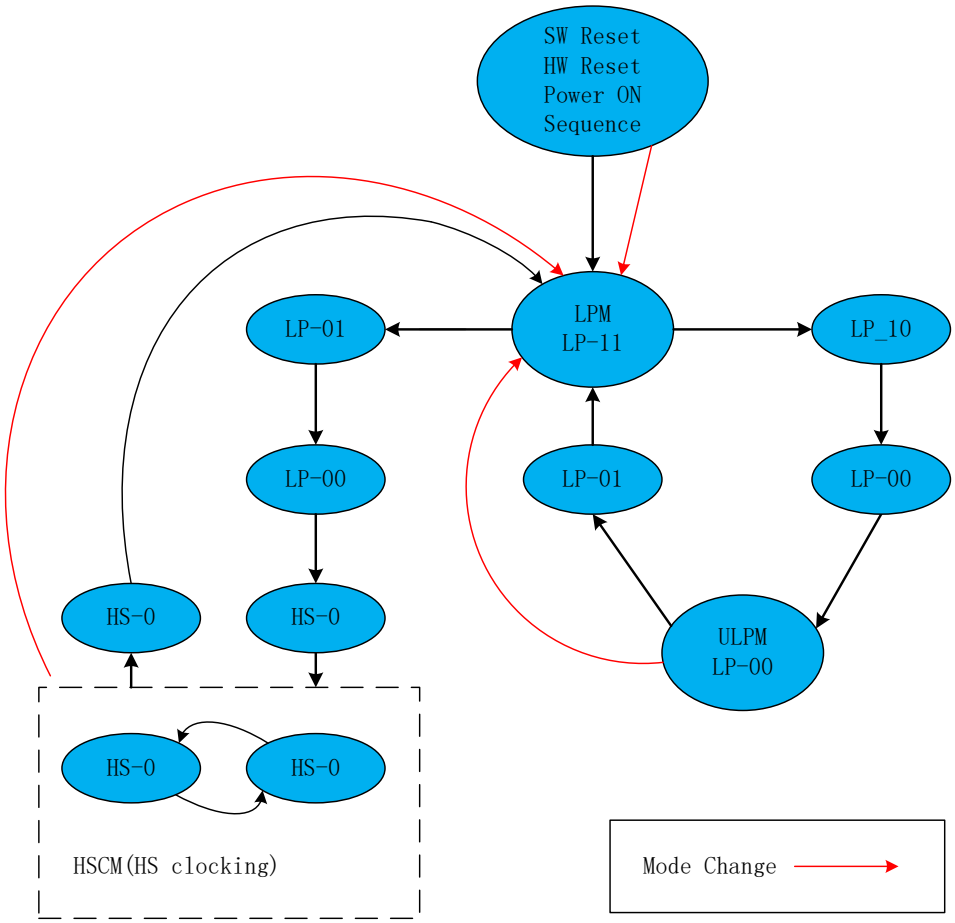
2) After DK_P/N lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.



3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence is illustrated below.



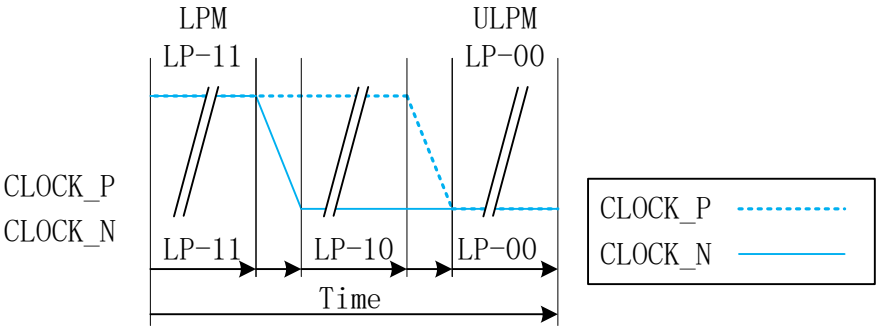
All three mode changes are illustrated a flow chart below.



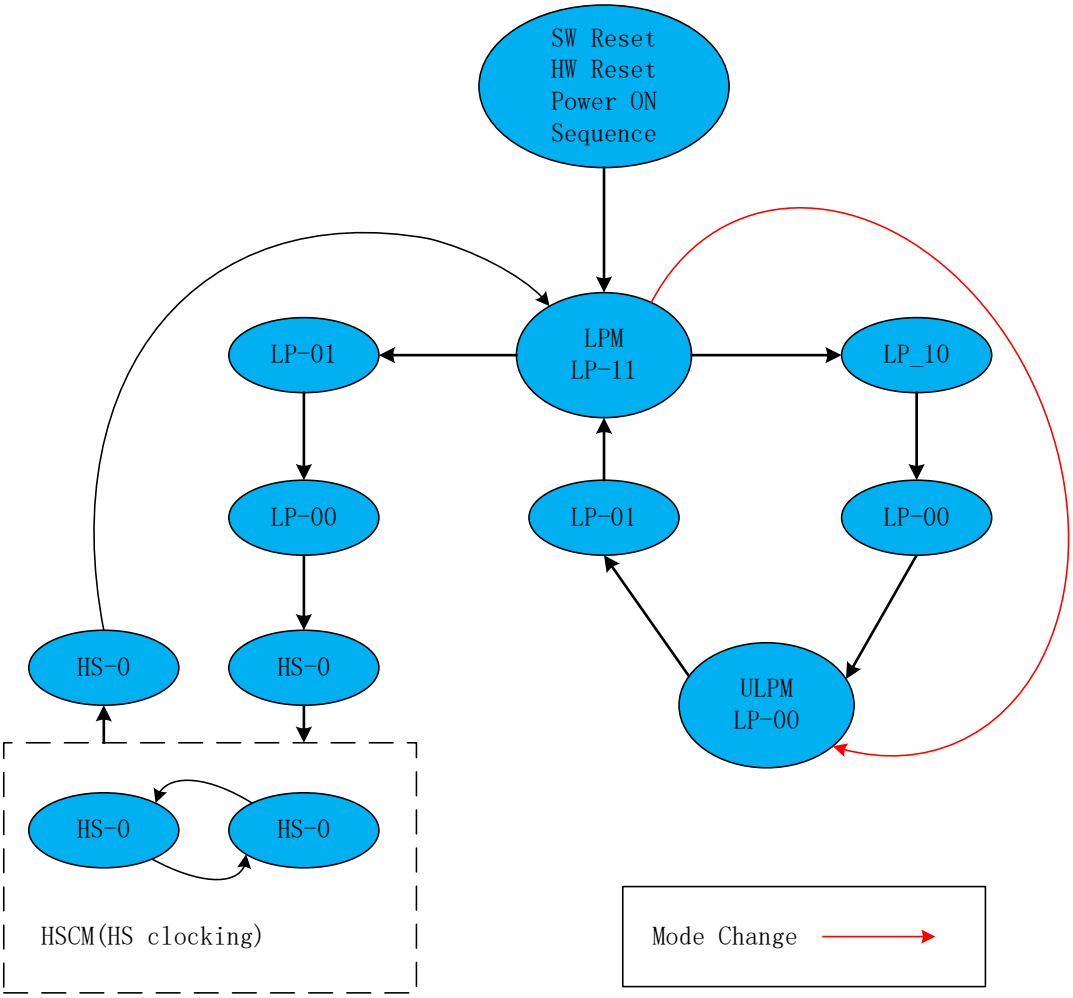
3.4.1.2 Ultra Low Power Mode (ULPM)

DK_P/N lanes can be driven to the Ultra Low power Mode (ULPM), when DK lanes are entering LP-00 State Code.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10 =>LP-00 (ULPM). This sequence is illustrated below



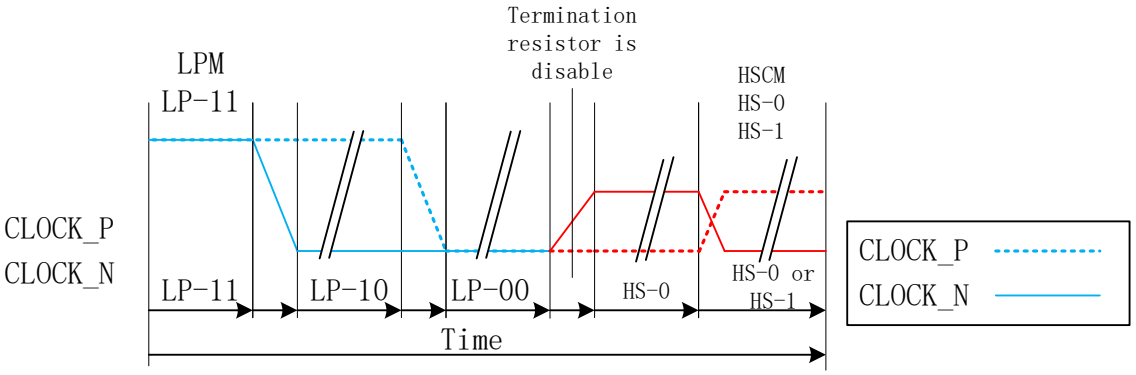
The mode change is also illustrated below.



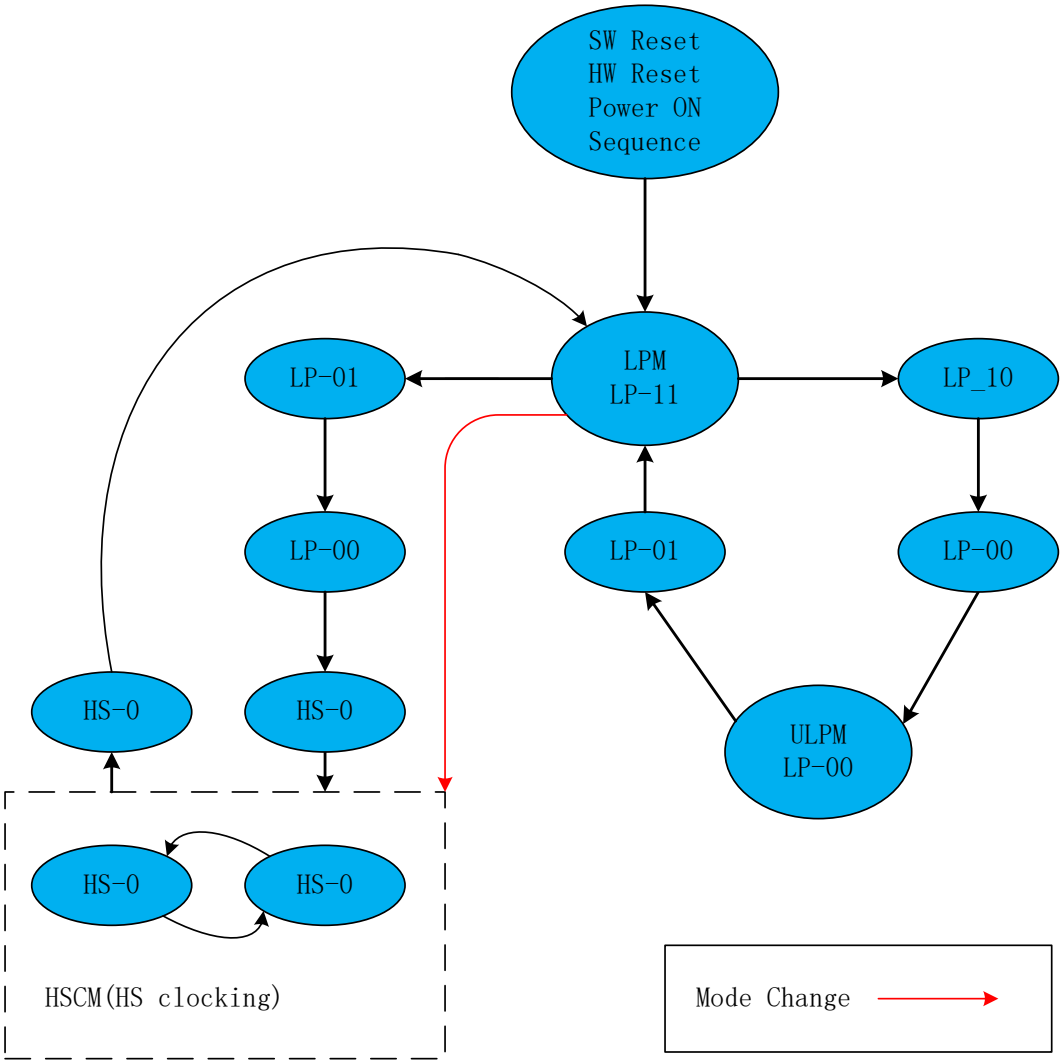
3.4.1.3. High-Speed Clocked Mode (HSCM)

DK_P/N lanes can be driven to the High Speed Clock Mode (HSCM), when DK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

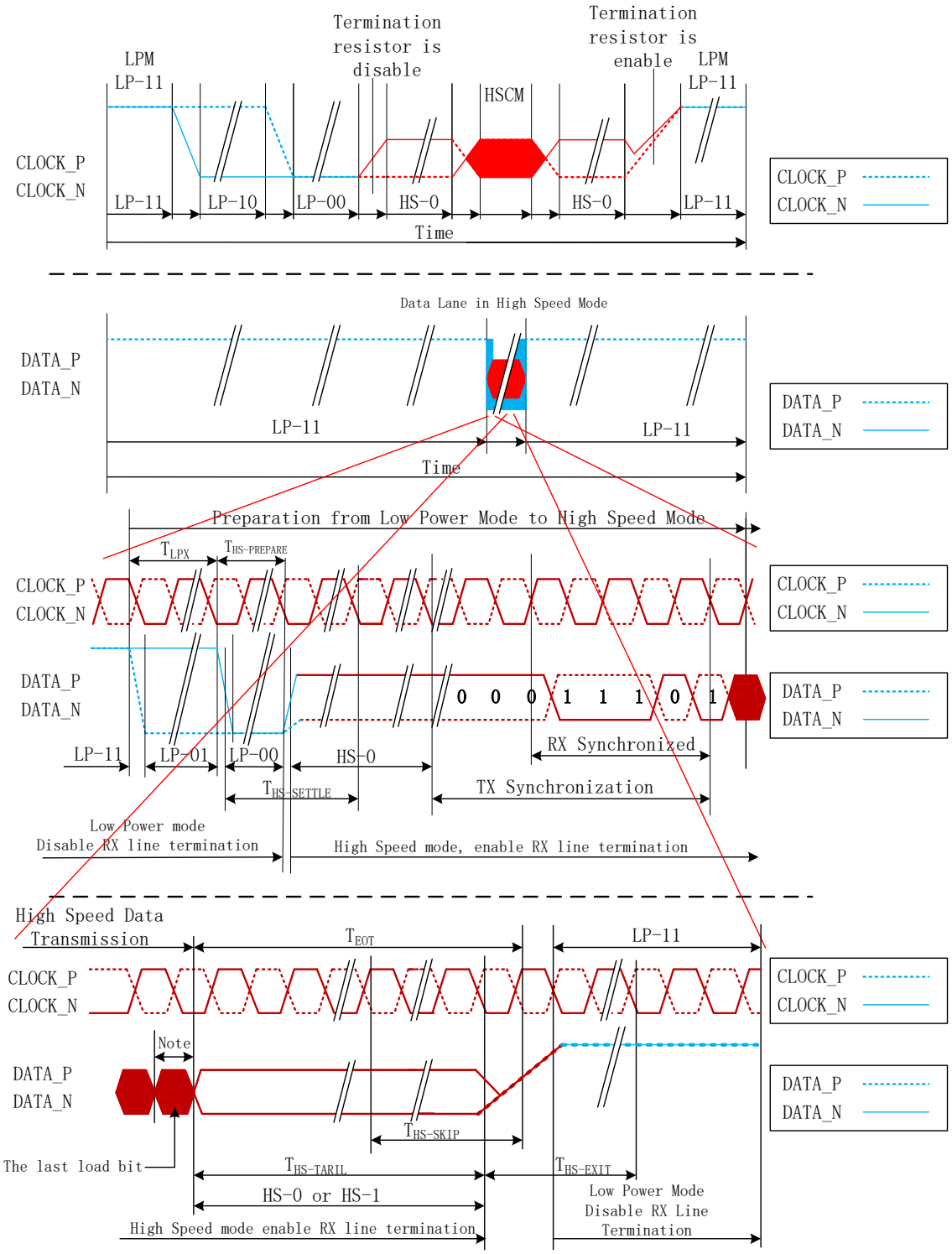


The mode change is also illustrated below.



The high speed clock (DK_P/N) is started before high speed data is sent via DK_P/N lanes. The high speed clock continues clocking after the high speed data sending has been stopped. The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0



Notes: 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

3.4.2. Interface Level Communication – Data Lanes

D0_P/N Data Lanes can be driven in different modes which are:

- Escape Mode
- High-Speed Data Transmission
- Bus Turnaround Request

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 → LP-10 → LP-00 →LP-01 →LP-00	LP-00 →LP-10 →LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 →LP-01 →LP-00 →HS-0	(HS-0 or HS-1) →LP-11
Bus Turnaround Request	LP-11 →LP-10 →LP-00 →LP-10 →LP-00	Hi-Z

3.4.2.1 Escape Modes

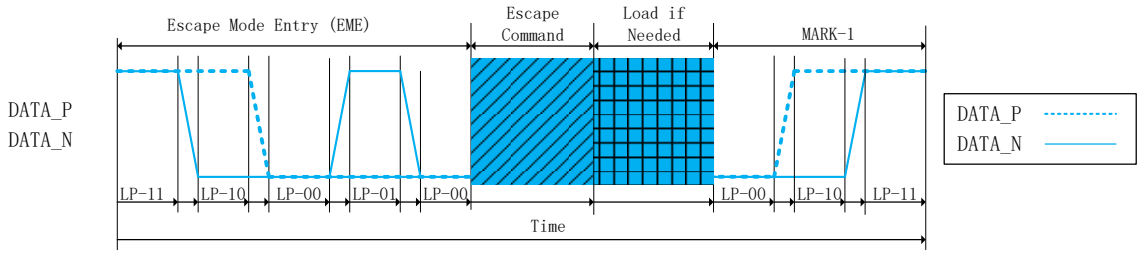
Data lanes (D0_P/N) can be used in different Escape Modes when data lanes are in Low Power (LP) mode. These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to GC9B71,
- Drive data lanes to “Ultra-Low Power State” (ULPS),
- Indicate “Remote Application Reset” (RAR), which is resetting GC9B71,
- Indicate “Tearing Effect” (TEE), which is used for a TE line event from GC9B71 to the MCU,
- Indicate “Acknowledge” (ACK), which is used for a non-error event from GC9B71 to the MCU

The basic sequence of the Escape Mode is as follow:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-DATA_P = 1, DSI-DATA_N- = 0) e.g. When DSI-DATA_N is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

This basic construction is illustrated below:



There are a total of eight Escape Command(EC) divided into two types, Modes and Triggers(see below table).
An example of a Mode type Escape Command is “Ultra-Low Power Mode” where the MCU instructs the display module to enter it’s Ultra-Low Power Mode.
An example of Trigger type Escape Command is ‘Tearing Effect’. In this case the MCU has already instructed .The display module to provide this trigger and is waiting for the response. The display module then sends a TE Trigger(TEE) on the next V-sync event.

Escape commands are defined on the next table.

Escape command	Command Type Mode / Trigger	Entry command Pattern (First to Last Bit Transmitted)
Low-Power Data Transmission	Mode	1110 0001
Ultra-Low Power Mode	Mode	0001 1110
Undefined-1, Note	Mode	1001 1111
Undefined-2, Note	Mode	1101 1110
Remote Application Reset	Trigger	0110 0010
Tearing Effect	Trigger	0101 1101
Acknowledge	Trigger	0010 0001
Uknown-5, Note	Trigger	1010 0000

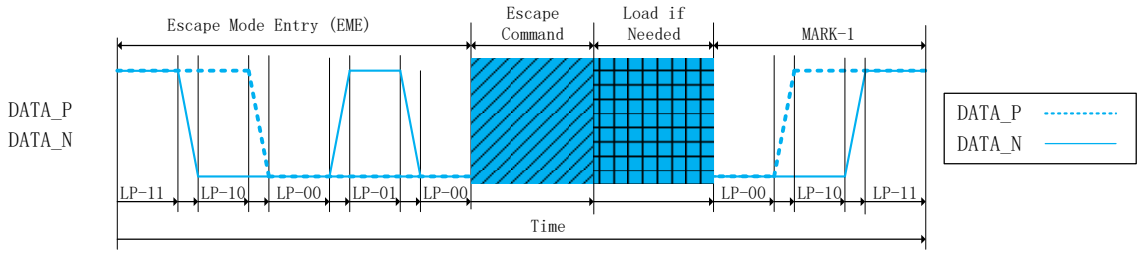
Note: This Escape command support has not been implemented on GC9B71.

3.4.2.1.1. Low-Power Data Transmission (LPDT)

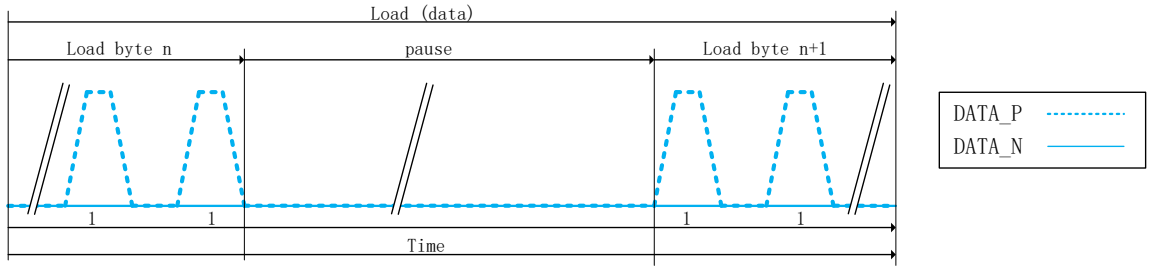
The MCU can send data to GC9B71 in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to GC9B71. GC9B71 is also using the same sequence when it is sending data to the MCU.
The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data):
  - One or more bytes (8 bit)
  - Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Note: Load (Data) is presenting that the first bit is logical ‘1’ in this example.



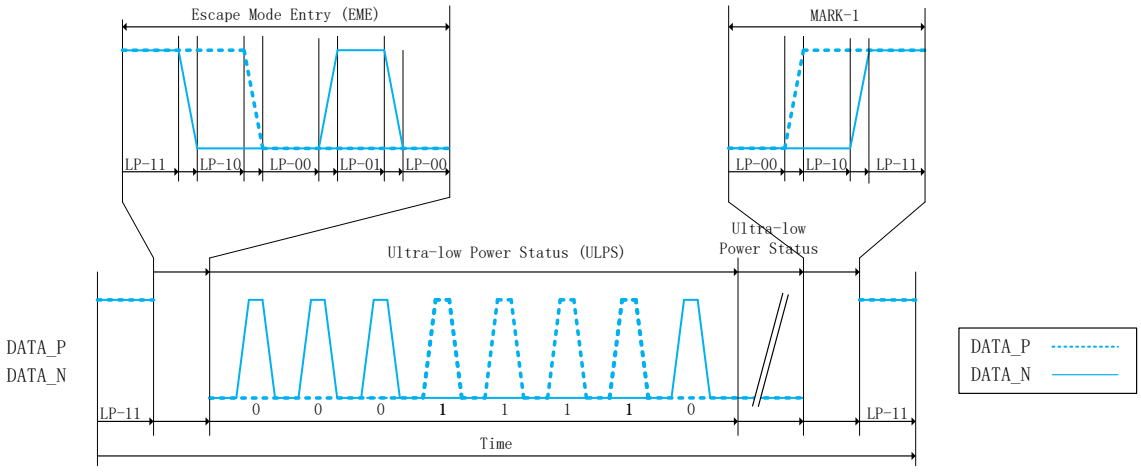
3.4.2.1.2. Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



3.4.2.1.3. Remote Application Reset (RAR)

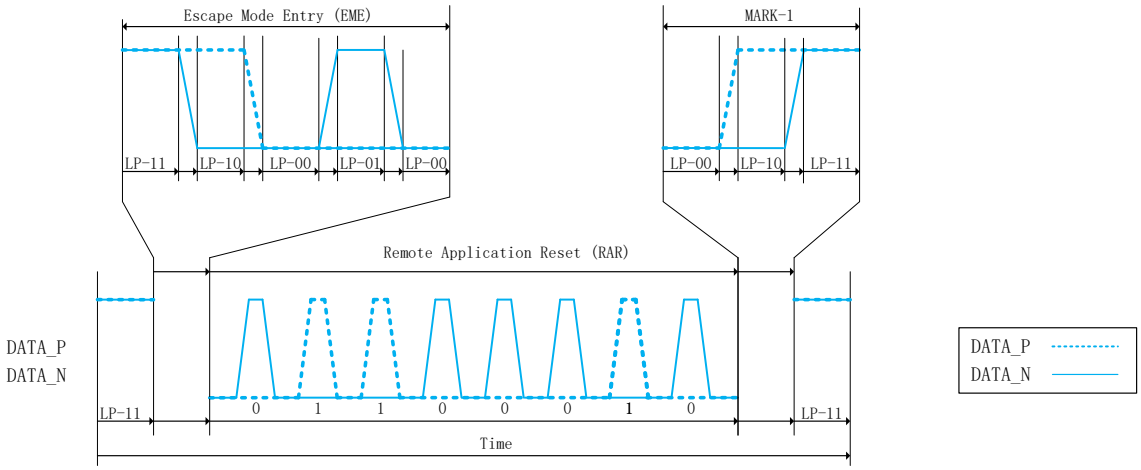
The MCU can inform to GC9B71 that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)

- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

- This sequence is illustrated for reference purposes below:



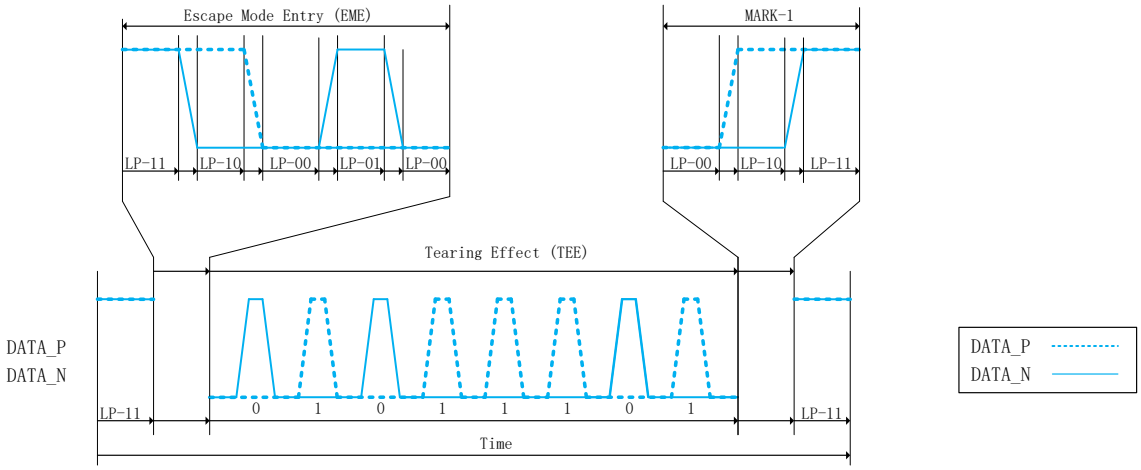
3.4.2.1.4. Tearing Effect (TEE)

GC9B71 can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



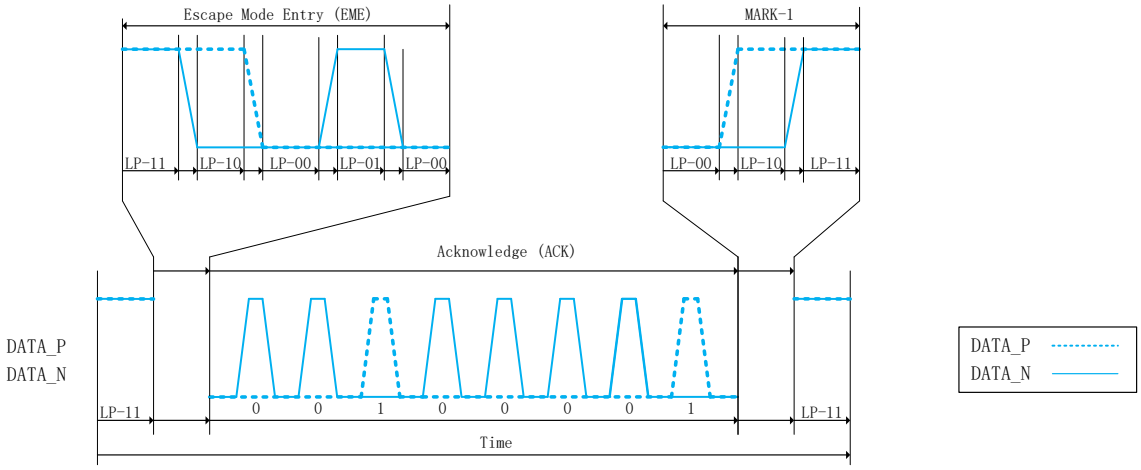
3.4.2.1.5. Acknowledge (ACK)

GC9B71 can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The display module is sending the Acknowledge (ACK) what is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



3.4.2.2. High-Speed Data Transmission (HSDT)

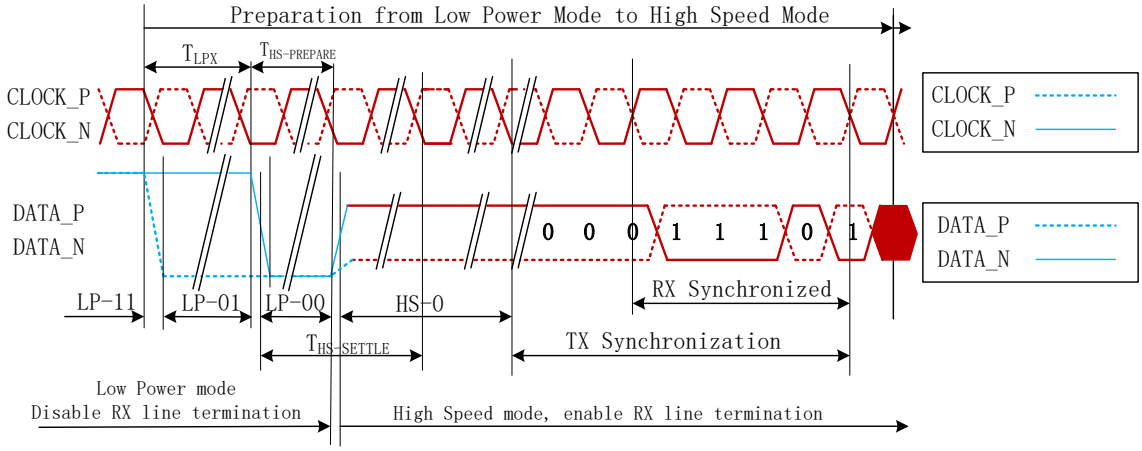
3.4.2.2.1. Entering High-Speed Data Transmission (TSOT of HSDT)

GC9B71 is entering High-Speed Data Transmission (HSDT) when Clock lanes DK_P/N have already been entered in the High-Speed Clock Mode (HSCM) by the MCU.

Data lanes DSI-DATA_P/N of GC9B71 are entering (TSOT) in the High-Speed Data Transmission (HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below:



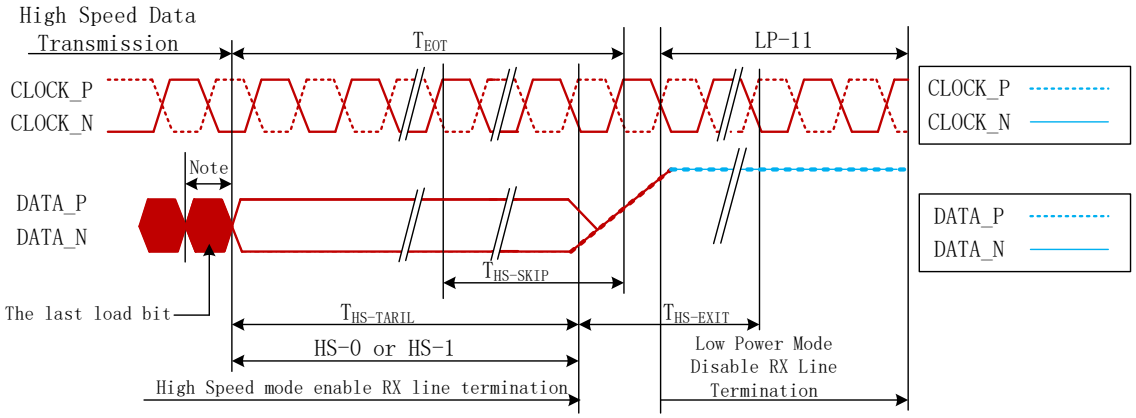
3.4.2.2.2. Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

GC9B71 is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DK_P/N are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes DSI-DATA_P/N are in LP-11 mode.

Data lanes DSI-DATA_P/N of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
  - MCU changes to HS-1, if the last load bit is HS-0
  - MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below

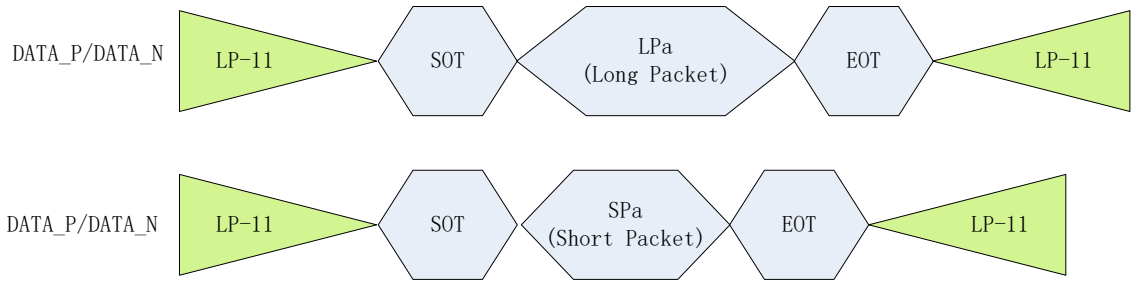


Note: 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

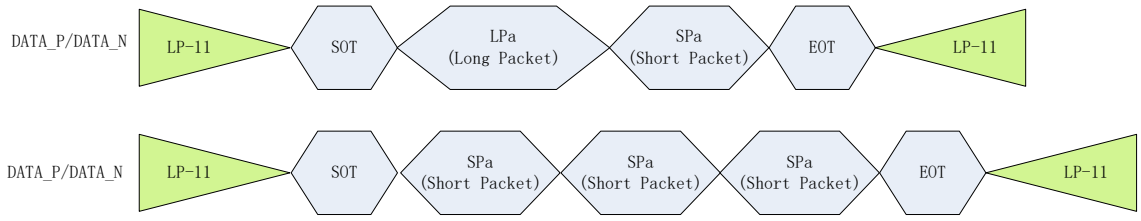
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

3.4.2.2.3.Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter “4.3.3.1 Short Packet (SPa) and Long Packet (LPa) Structures“.
The single packet in High-Speed Data Transmission is illustrated for reference purposes below:



The multiple packets in High-Speed Data Transmission are illustrated for reference purposes below:



Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes are ‘1’s (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

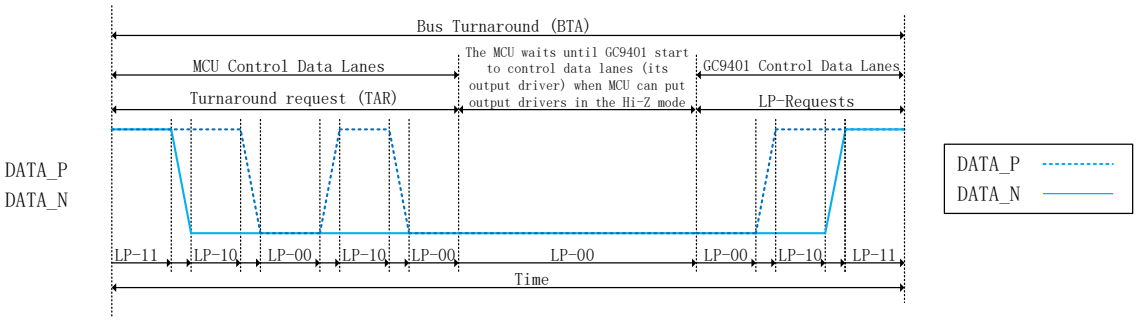
3.4.2.3.Bus Turnaround (BTA)

The MCU or GC9B71, which is controlling DSI-DATA_P/N Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or GC9B71. The MCU and GC9B71 are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to GC9B71, as follows.

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 =>LP-10 =>LP-00=>LP-10=>LP-00
- The MCU waits until GC9B71 is starting to control DSI-DATA_P/N data lanes and the MCU stops to control DSI-DATA_P/N data lanes (= High-Z)

- GC9B71 changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the MCU to GC9B71) is illustrated below:



3.4.3.Packet Level Communication

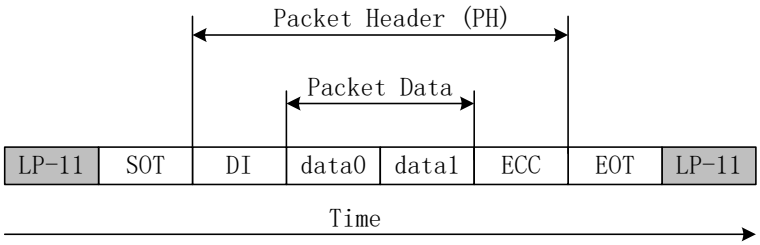
3.4.3.1. Short Packet and Long Packet Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are：

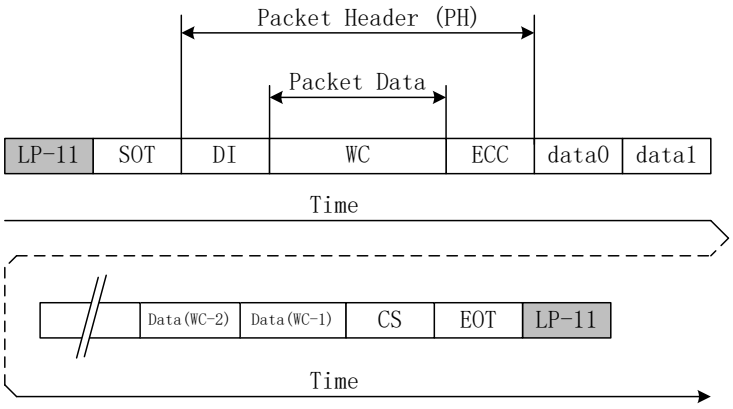
- Short Packet (SPa): 4 bytes
- Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH). The Short Packet structure is illustrated as below:



LP-11: low power -Stop State
SOT: Start of Transmisstion
DI: 8-bit data Identification
Data0/data1: 8-bit packet data
ECC: 8-bit Error cerrection code
EOT: End of Transmisstion

The Long Packet structure is illustrated as below:



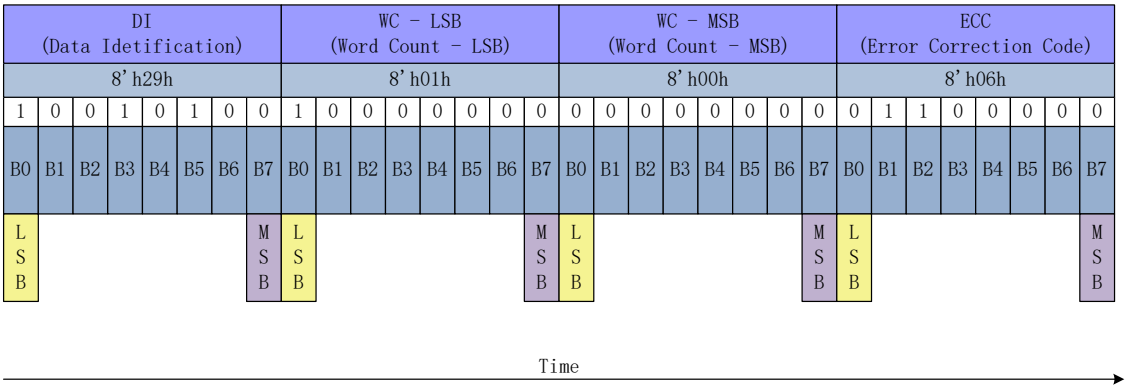
LP-11: low power -Stop State
SOT: Start of Transmisstion
DI: 8-bit data Identification
WC: 16-bit word count(0-65535)
ECC: 8-bit Error cerrection code
Data0/…/Data(WC-1): 8-bit packet data
CS: 16-bit, the Check Sum = Packet Footer(PF)
EOT: End of Transmisstion

The other possibility is that there is not needed SOT, EOT and LP-11 between packets if packets have sent in multiple packet format e.g.

- LP-11 =>SOT =>SPa =>LPa =>SPa =>SPa =>EOT =>LP-11
- LP-11 =>SOT =>SPa =>SPa =>SPa =>EOT =>LP-11
- LP-11 =>SOT =>LPa =>LPa =>LPa =>EOT =>LP-11

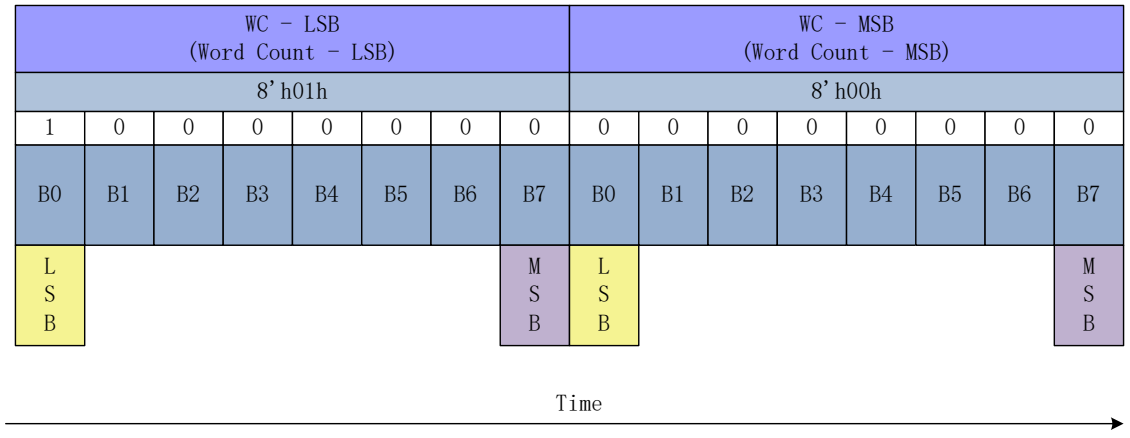
3.4.3.1.1. Bit Order of the Byte on Packets

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last.
This same order is illustrated for reference purposes below.



3.4.3.1.2. Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.
This same order is illustrated for reference purposes below.

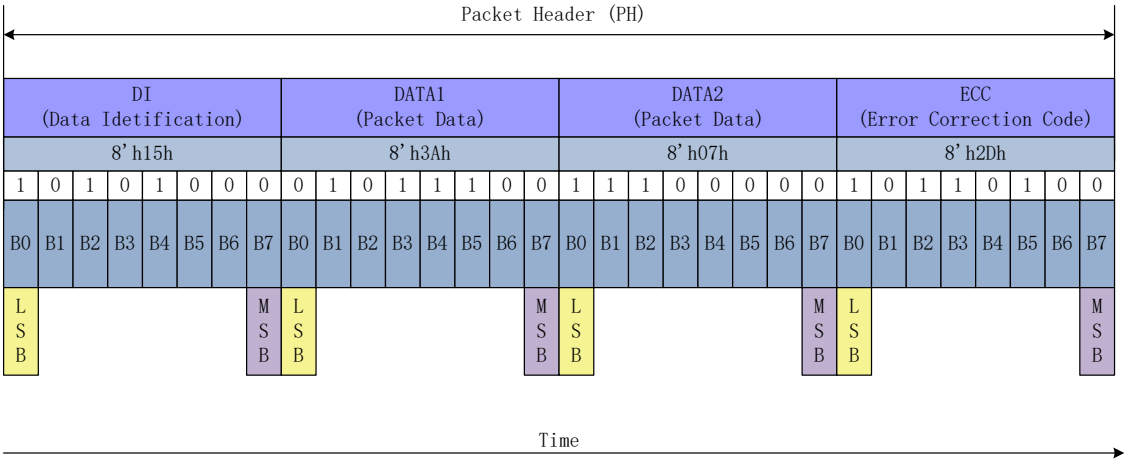


3.4.3.1.3. Packet Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

- 1_{st} byte: Data Identification (DI) => Identification that this is Short Packet (SPa)
- 2_{nd} and 3_{rd} bytes: Packet Data (PD), Data 0 and 1
- 4_{th} byte: Error Correction Code (ECC)



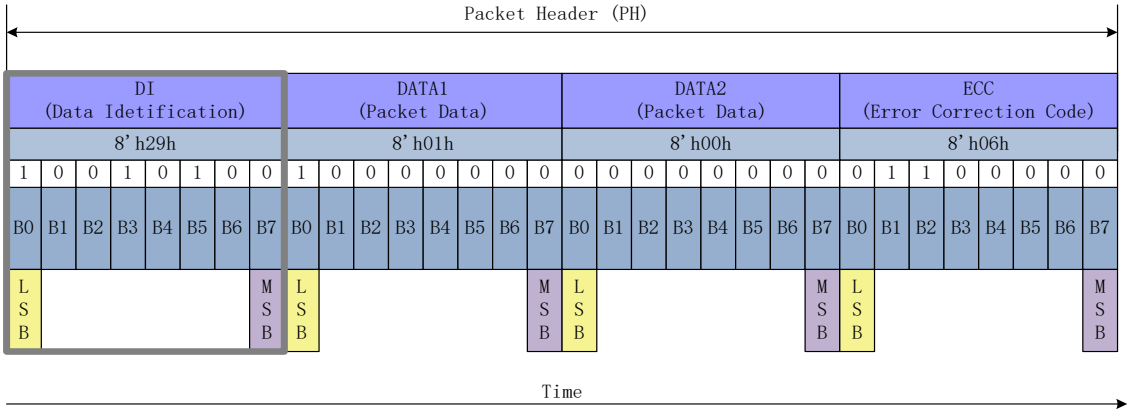
3.4.3.1.4. Data Identification (DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI [7...6]
- Data Type (DT), 6 bits, DI [5…0]

The Data Identification (DI) structure is illustrated on a diagram below.

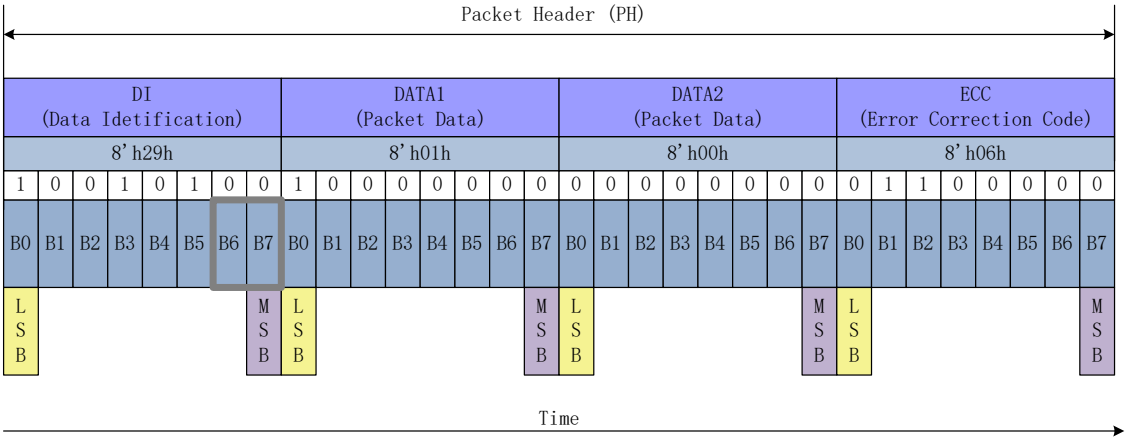

B7 B6 B5 B4 B3 B2 B1 B0
VC
DT
Virture Channel Identifier(VC)
Data Type (DT)


Packet Header (PH)
DI (Data Idetification)
DATA1 (Packet Data)
DATA2 (Packet Data)
ECC (Error Correction Code)
8'h29h
8'h01h
8'h00h
8'h06h
1 0 0 1 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0
B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7
LSB MSB LSB MSB LSB MSB LSB MSB
Time

3.4.3.1.4.1. Virtual Channel (VC)

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals. The Virtual Channel ID enables one serial stream to service two or more virtual peripherals by multiplexing packets onto a common transmission channel. Note that packets sent in a single transmission each have their own Virtual Channel assignment and can be directed to different peripherals.

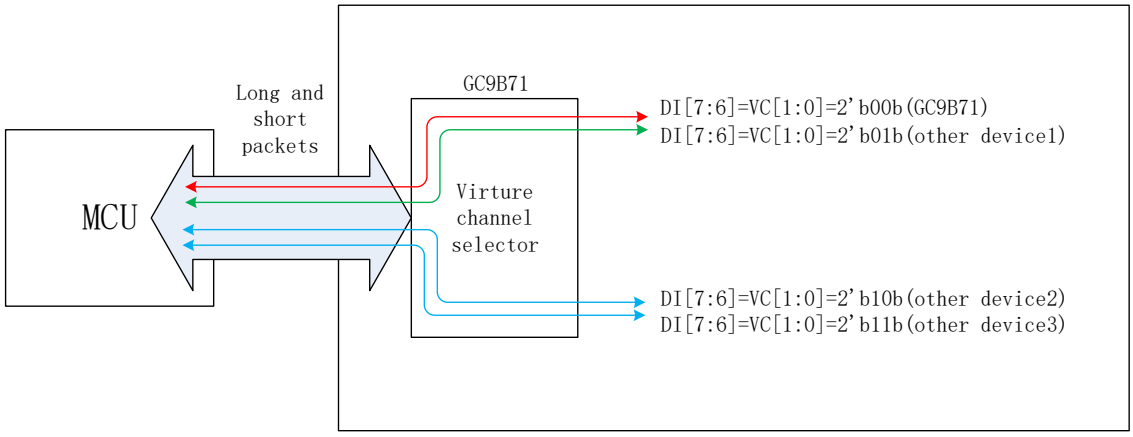
Virtual Channel (VC) is a part of Data Identification (DI [7…6]) structure and it is used to address where a packet is wanted to send from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.



Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MCU is using to send packets to them e.g.

- The MCU is using the virtual channel 0 when it sends packets to this display module
- This display module is also using the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.



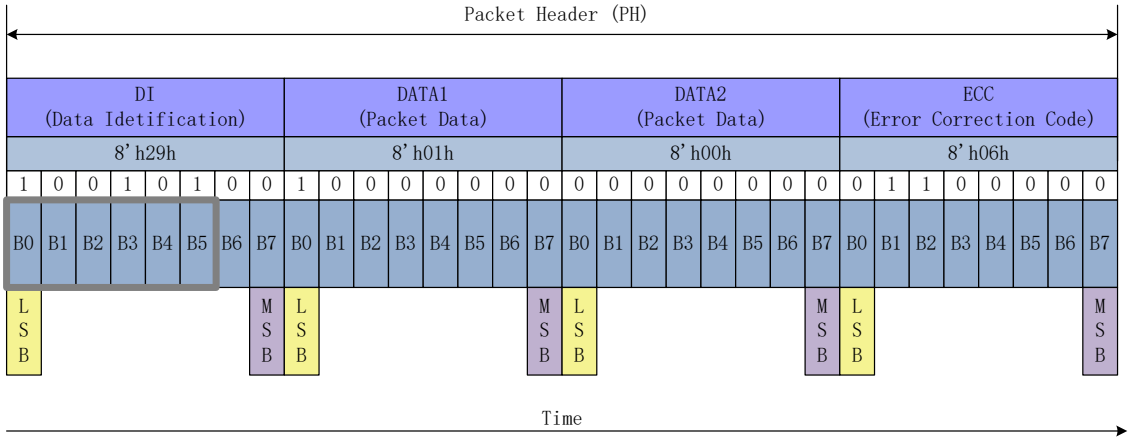
Virtual Channel (VC) is always 0 (DI[7..6]=VC[1..0]=00b) when the MCU is sending "End of Transmission Packet" to the display module.

3.4.3.1.4.2. Data Type (DT)

The Data Type field specifies if the packet is a Long or Short packet type and the packet format. The Data Type field, along with the Word Count Field for Long Packets, informs the receiver of how many bytes to expect in the remainder of the packet. This is necessary because there are no special packet start/end sync codes to indicate the beginning and end of a packet. This permits packets to convey arbitrary data, but it also requires the packet header to explicitly specify the size of the packet.

When the receiving logic has counted down to the end of a packet, it shall assume the next data is either the header of a new packet or the EoT (End of Transmission) sequence.

Data Type (DT) is a part of Data Identification (DI [5…0]) structure and it is used to define a type of the used data on a packet. Bits of the Data Type (DT) are illustrated for reference purposes below.



This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Type (DT) are defined on tables below

From the MCU to GC9B71									
B5	B4	B3	B2	B1	B0	Hex	Description	Short/Long Packet	Abbreviation
0	0	1	0	0	0	08	End of Transmission Packet, Note1	Spa (Short Packet)	EOTP
0	0	0	1	0	1	05	DCS Write, No Parameter	SPa (Short Packet)	DCSWN-S
0	1	0	1	0	1	15	DCS Write, 1 Parameter	SPa (Short Packet)	DCSW1-S
0	0	0	1	1	0	06	DCS Read, No Parameter	SPa (Short Packet)	DCSRN-S
1	1	0	1	1	1	37	Set Maximum Return Packet Size	SPa (Short Packet)	SMRPS-S
0	0	1	0	0	1	09	Null Packet, No Data, Note2	LPa (Long Packet)	NP-L
1	1	1	0	0	1	39	DCS Write Long	LPa (Long Packet)	DCSW-L

Notes: 1. This can be used when the MCU wants to secure that there is the end of the transmission in High

Speed Data Transferring (HSDT) mode.

2. This can be used when data lanes are wanted to keep in High Speed Data Transferring (HSDT) Mode.
3. The receiver is ignored other Data Type (DT) if they are not defined on tables.

From the GC9B71 to MCU									
B5	B4	B3	B2	B1	B0	Hex	Description	Short/Long Packet	Abbreviation
0	0	0	0	1	0	02	Acknowledge with Error Report	Spa (Short Packet)	AwER
0	1	1	1	0	0	1C	DCS Read Long Response	LPa (Long Packet)	DCSRR-L
1	0	0	0	0	1	21	DCS Read Short Response, 1 byte returned	SPa (Short Packet)	DCSRR1-S
1	0	0	0	1	0	22	DCS Read Short Response, 2 byte returned	SPa (Short Packet)	DCSRR2-S

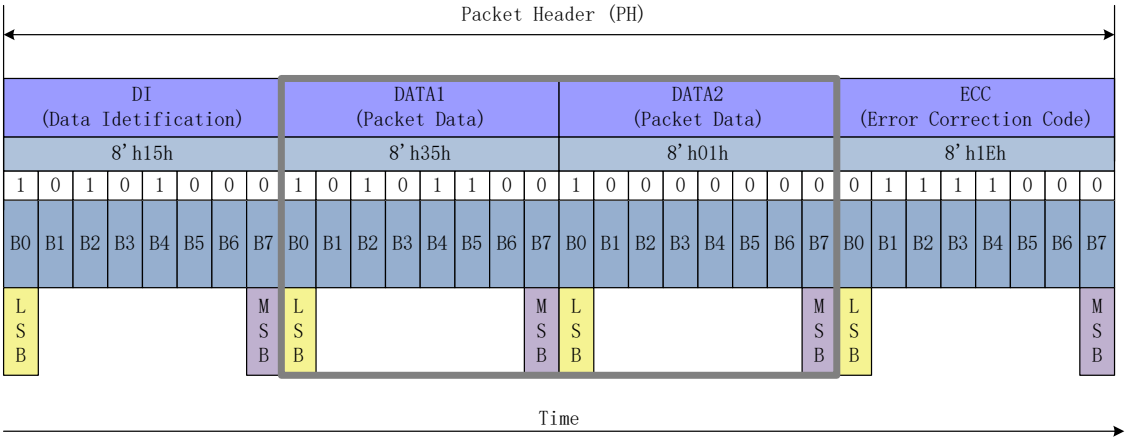
Notes: 1. The receiver is ignored other Data Type (DT) if they are not defined on tables.

3.4.3.1.4.3. Packet Data on the Short Packet

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send. Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1. Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last. Bits of Data 1 are set to '0' if the information length is 1 byte.
Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

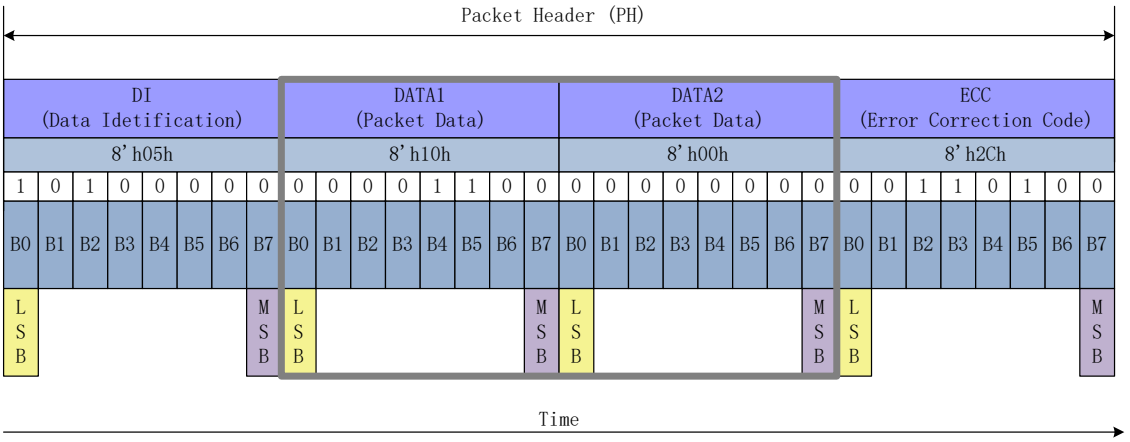
Packet Data (PD) information:

- Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI (Data Type (DT)) = 15hex)
- Data 1: 01hex (DCS's parameter)



Packet Data (PD) information:

- Data 0: 10hex (DCS without parameter => DI (Data Type (DT)) = 05hex)
- Data 1: 00hex (Null)



3.4.3.1.4.4.Word Count on the Long Packet

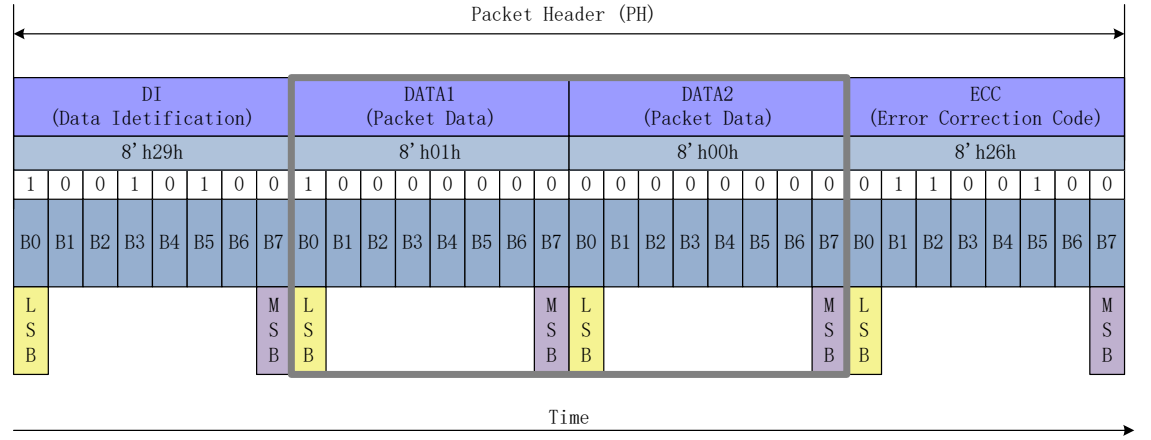
Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

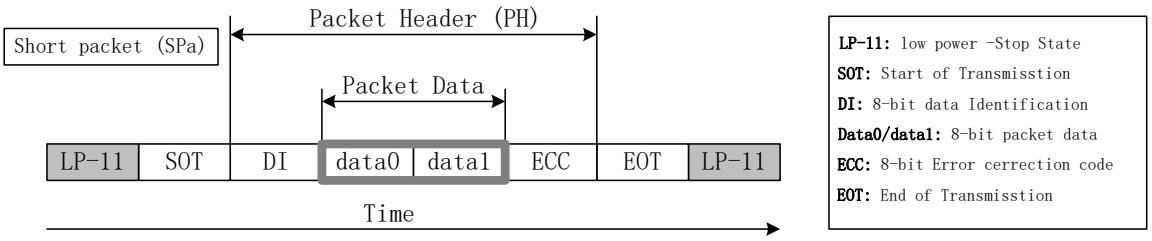
Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) are placed in the Packet Header (PH).

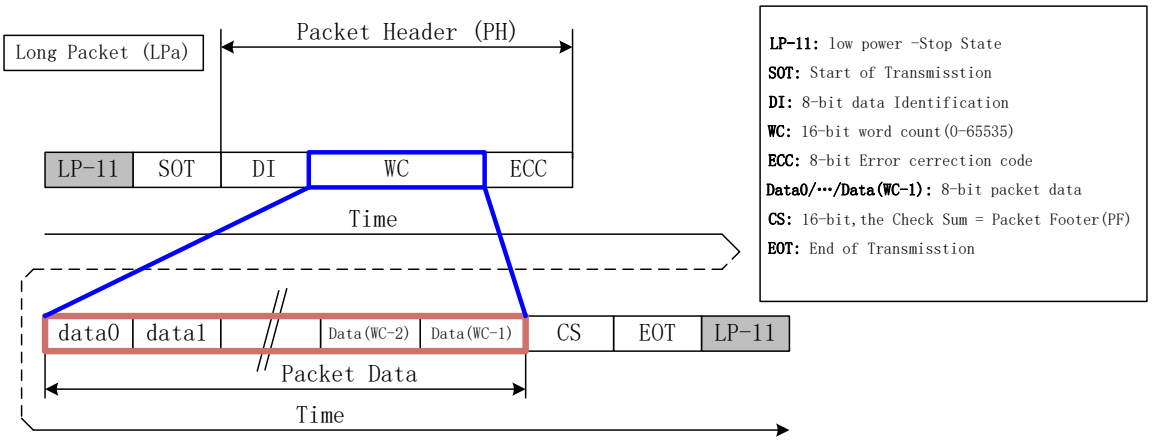
Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.







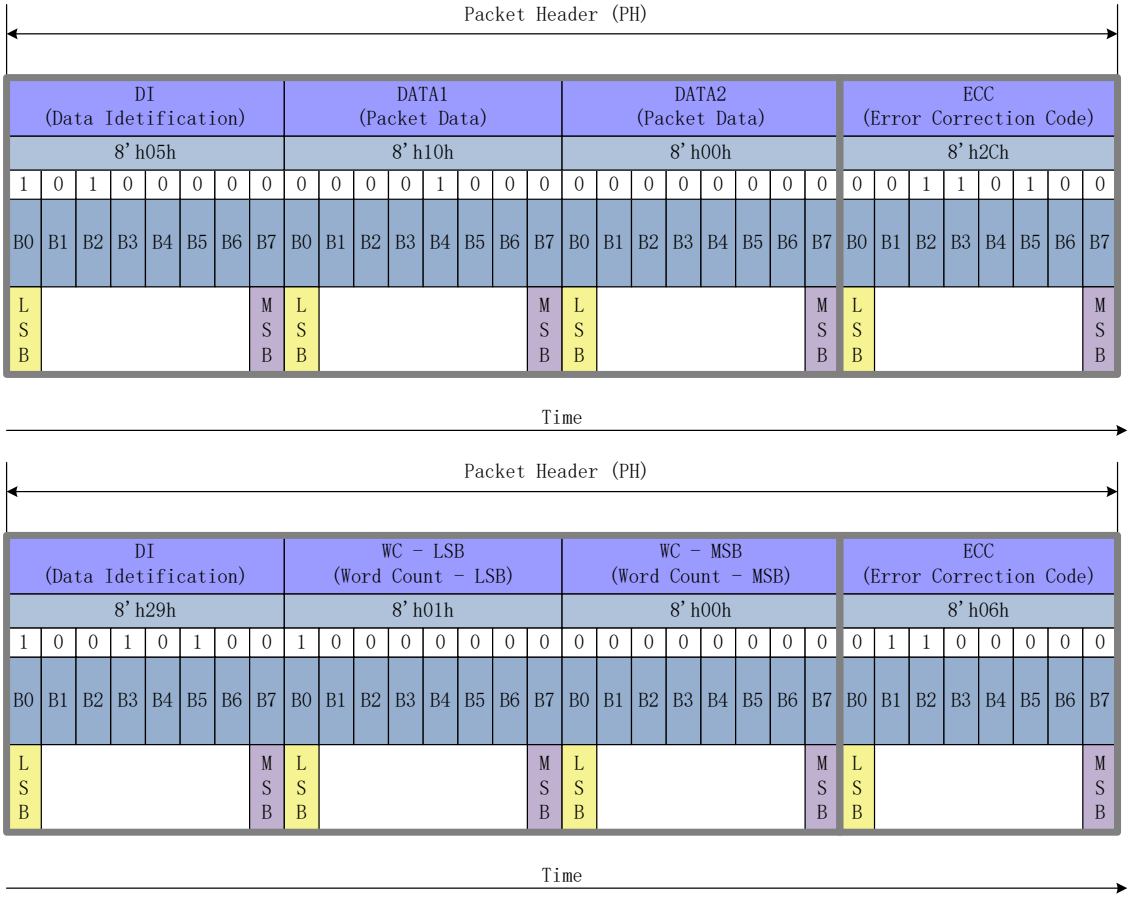
3.4.3.1.4.5. Error Correction Code (ECC)

The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. The host processor shall always calculate and transmit an ECC byte and GC9B71 supports ECC in both forward- and reverse-direction communications.

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors:

- Short Packet (SPa): Data Identification (DI) and Packet Data (PD) bytes (24 bits: D [23…0])
- Long Packet (LPa): Data Identification (DI) and Word Count (WC) bytes (24 bits: D [23…0])

D [23…0] is illustrated for reference purposes below.



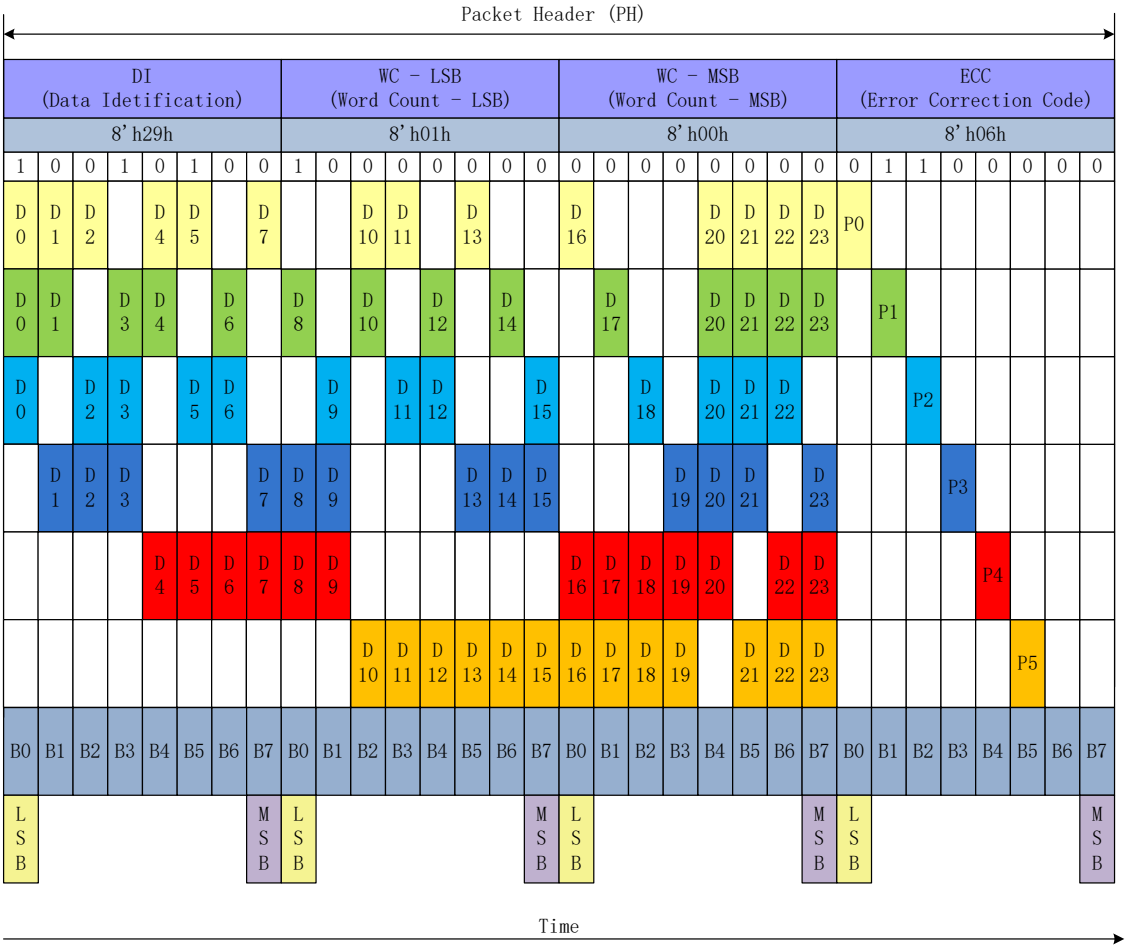
Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

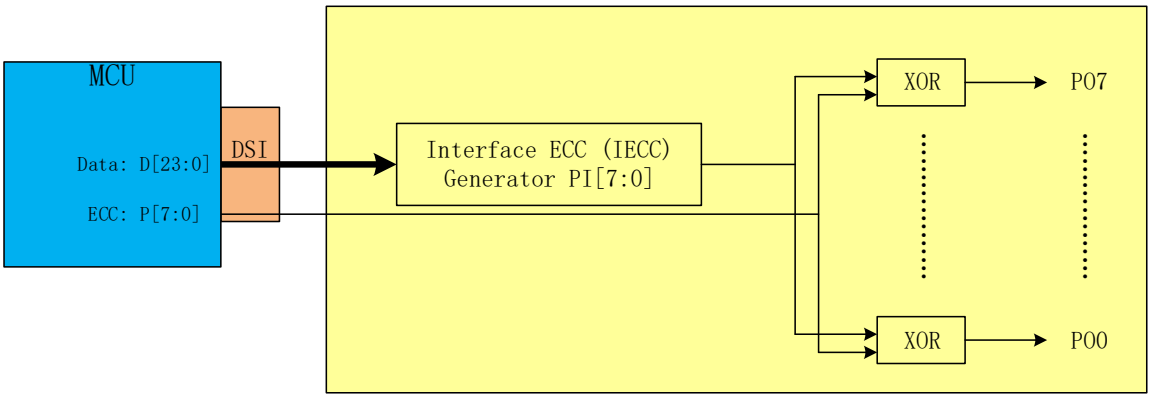
- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D [23…0]). Therefore, there is only needed 6 bits (P [5…0]) for Error Correction Code (ECC).



The transmitter (The MCU or GC9B71) is sending data bits D [23…0] and Error Correction Code (ECC) P [7…0]. The receiver (GC9B71 or the MCU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO [7…0]. This functionality, where the transmitter is the MCU and the receiver is GC9B71, is illustrated for reference purposes below.



The sent data bits (D[23…0]) and ECC (P[7…0]) are received correctly, if a value of the PO[7…0]) is 00h. The sent data bits (D[23…0]) and ECC (P[7…0]) are not received correctly, if a value of the PO[7…0]) is not 00h.

ECC P[7:0]	1	1	0	0	0	0	0	0	03h
IECC PI[7:0]	1	1	0	0	0	0	0	0	03h
(ECC) ⊕ (IECC) →PO[7:0]	0	0	0	0	0	0	0	0	=00h → No Error
	LSB							MSB	

ECC P[7:0]	1	1	0	0	0	0	0	0	03h
IECC PI[7:0]	1	1	1	1	0	0	0	0	0Fh
(ECC) ⊕ (IECC) →PO[7:0]	0	0	1	1	0	0	0	0	=0Ch → Error
	LSB							MSB	

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23…0] on the transmitter side. The number of the errors (one or more) can be defined when the value of the PO [7…0] is compared to values on the following table.

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch

D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

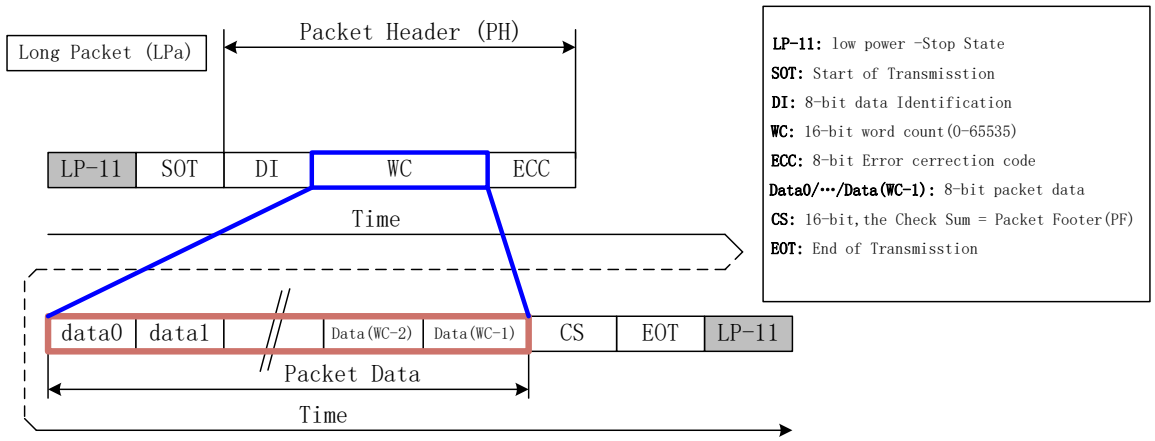
One error is detected if the value of the PO [7…0] is on the above table : One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

- PO [7…0] = 0Eh
- The bit of the data (D [23…0]), what is not correct, is D[3]

More than one error is detected if the value of the PO [7…0] is not on the above table: One Bit Error Value of the Error Correction Code (ECC) e.g. PO [7…0] = 0Ch.

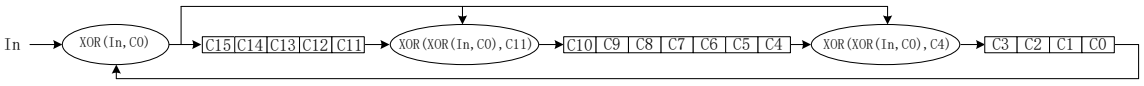
3.4.3.1.4.6. Packet Data on the Long Packet

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is illustrated as below:

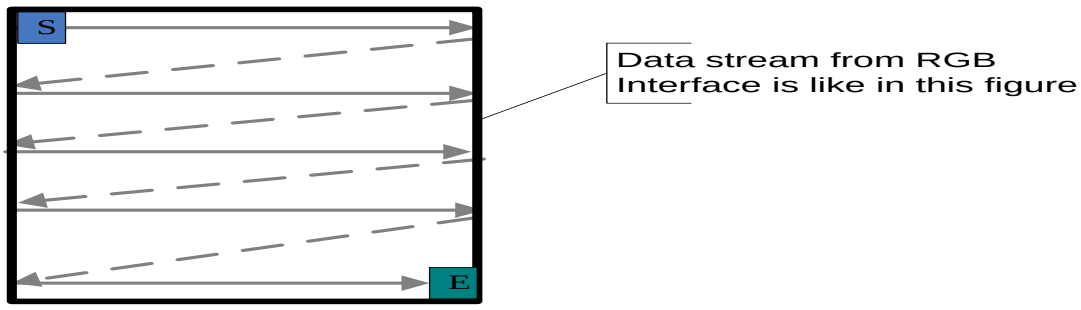


3.4.3.1.4.7. Packet Footer on the Long Packet

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa). The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial $X_{16}+X_{12}+X_5+X_0$ as it is illustrated below.

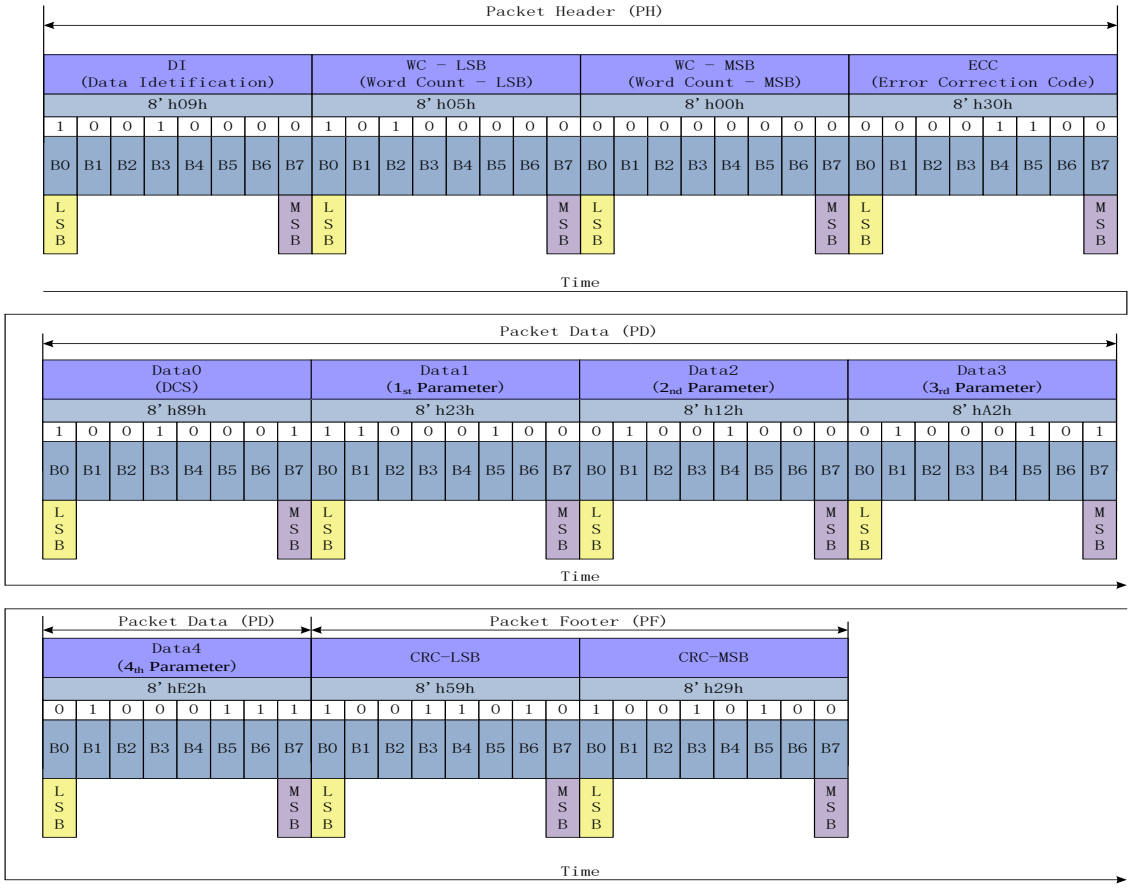


The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations.
The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).
An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is

illustrated below.



The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

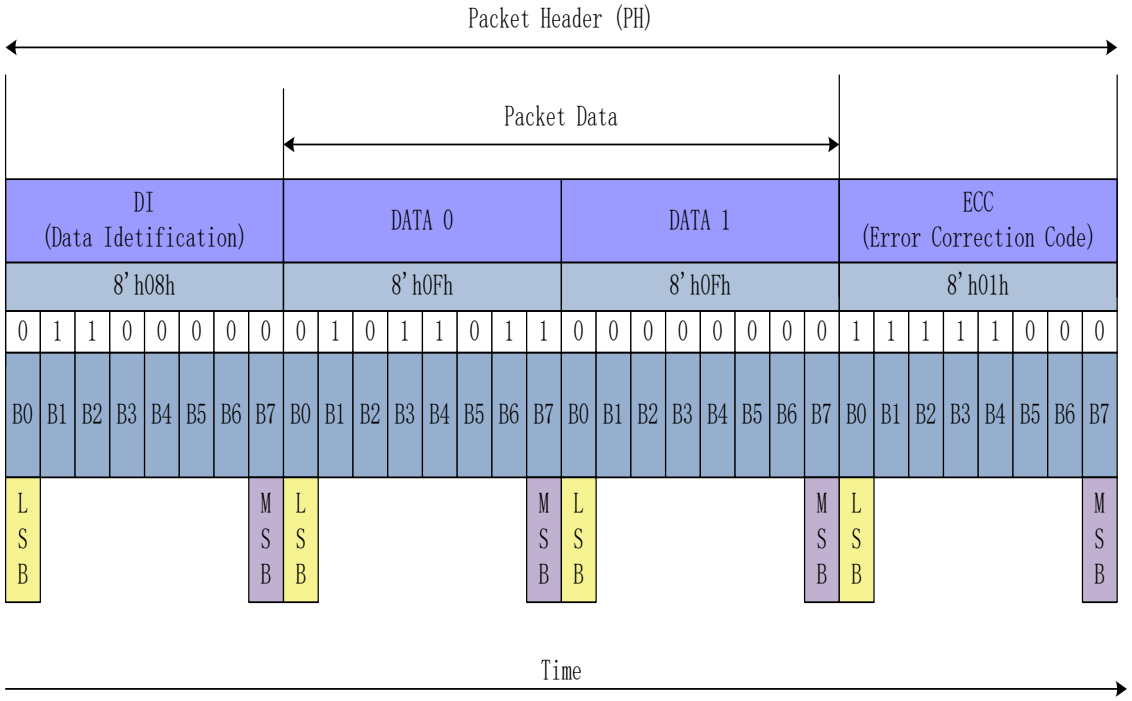
The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) is equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

3.5. Packet Transmissions

3.5.1. Packet form the MCU to GC9B71

3.5.1.1. Display Command Set (DCS)

Display Command Set (DCS), which is defined on next chapter, is used from the MCU to GC9B71. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated as below.



3.5.1.2. Display Command Set Write, no Parameter (DCSWN-S)

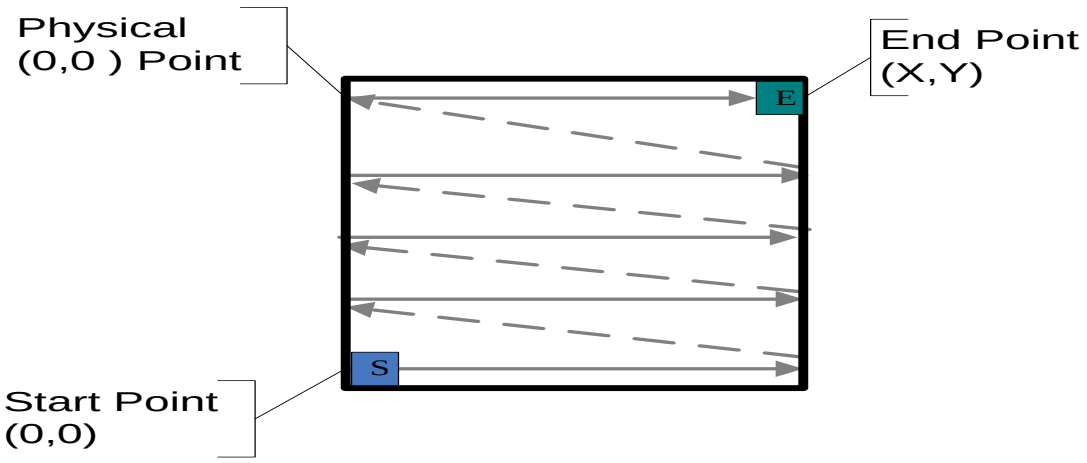
“Display Command Set (DCS) Write, No Parameter” is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MCU to GC9B71. These commands are defined on a table below.

Command
NOP (00h)
Software Reset (01h)
Sleep IN (10h)
Sleep Out (11h)
Partial Mode ON (12h)
Normal Display Mode ON (13h)
Display OFF (28h)
Display ON (29h)
Tearing Effect Line OFF (34h)
Idle Mode OFF (38h)
Idle Mode ON (39h)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 0101b
- Packet Data (PD)
  - Data 0: “Sleep In (10h)”, Display Command Set (DCS)
  - Data 1: Always 00hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



3.5.1.3.Display Command Set Write, 1 Parameter (DCSW1-S)

“Display Command Set (DCS) Write, 1 Parameter” (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MCU to GC9B71. These commands are defined on a table below.

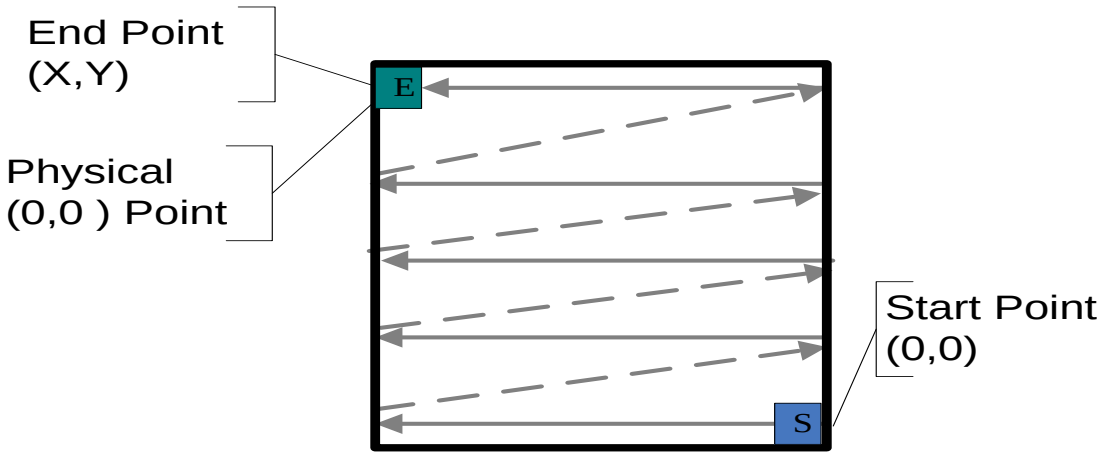
Command
Memory Write (2Ch), Note
Tearing Effect Line ON (35h)
Memory Access Control (36h)
Interface Pixel Format (3Ah)
Partial Mode ON (12h)
Memory Write Continue (3Ch), Note
Write Display Brightness (51h)
Write CTRL Display (53h)
Tearing Effect Line OFF (34h)
Write Content Adaptive Brightness control (55h)
Write CABC Minimum Brightness (5Eh)

Note: One Subpixel has been written

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 01 0101b
- Packet Data (PD)
  - Data 0: “Interface Pixel Format (3Ah)”, Display Command Set (DCS)
  - Data 1: 55hex, Parameter of the DCS.
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



3.5.1.4.Display Command Set Write Long (DCSW-L)

"Display Command Set (DCS) Write Long" (DCSW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 11 1001b), from the MCU to GC9B71. Command (No Parameters) and Write (1 or more parameters) are defined on a table below.

Command
NOP (00h), Note 1
Software Reset (01h), Note 1
Sleep IN (10h) , Note 1
Sleep Out (11h) , Note 1
Partial Mode ON (12h) , Note 1
Normal Display Mode ON (13h) , Note 1
Display OFF (28h) , Note 1
Display ON (29h) , Note 1
Column Address Set (2Ah)
Page Address Set (2Bh)
Memory Write (2Ch), Note 2
Partial Area (30h)
Tearing Effect Line OFF (34h), Note 1
Tearing Effect Line ON (35h), Note 2
Memory Access Control (36h), Note 2
Idle Mode OFF (38h) , Note 1
Idle Mode ON (39h) , Note 1
Interface Pixel Format (3Ah)
Memory Write Continue (3Ch), Note 2
Write Display Brightness (51h), Note 2
Write CTRL Display (53h) , Note 2
Write Content Adaptive Brightness control (55h) , Note 2
Write CABC Minimum Brightness (5Eh)

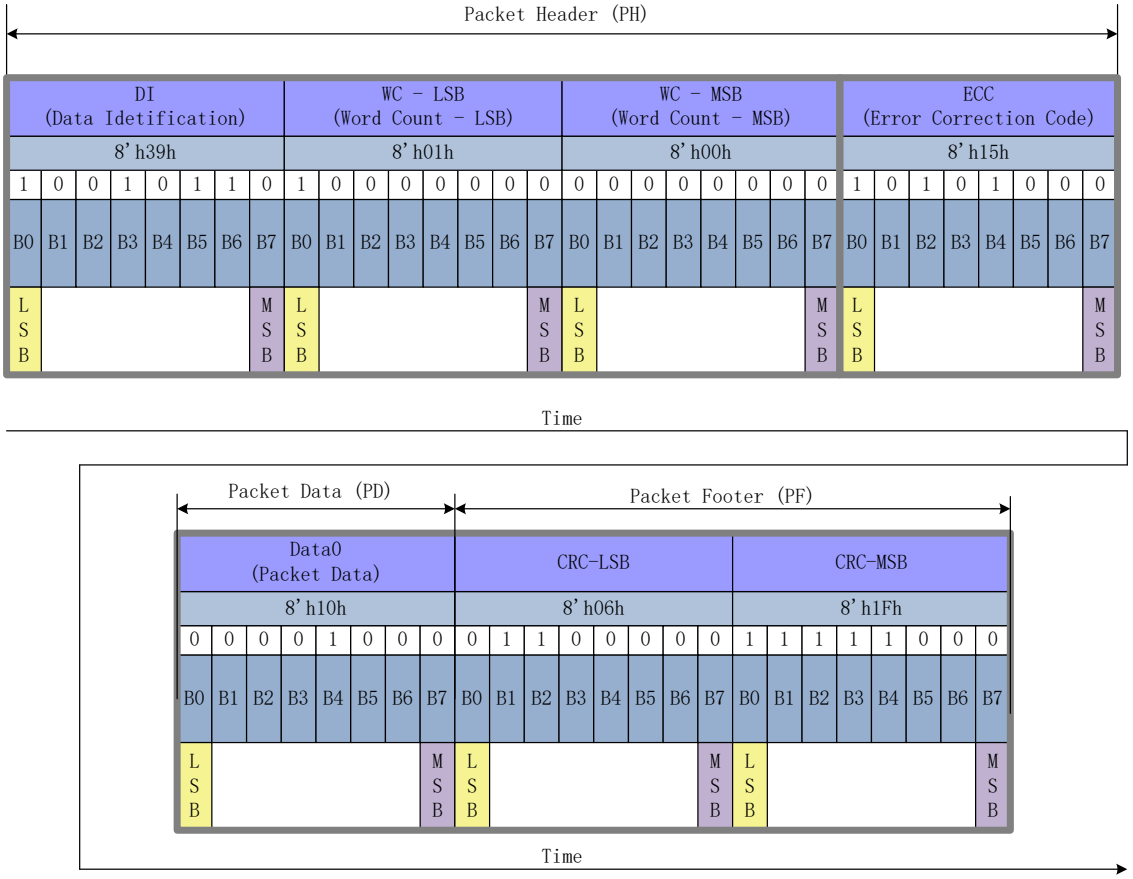
Notes: (1) Also Short Packet (SPa) can be used; See chapter "4.3.3.2.1.2 Display Command Set (DCS) Write, No Parameter"

(2) Also Short Packet (SPa) can be used; See chapter "4.3.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter"

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: "Sleep In (10h)", Display Command Set (DCS)
- Packet Footer (PF)

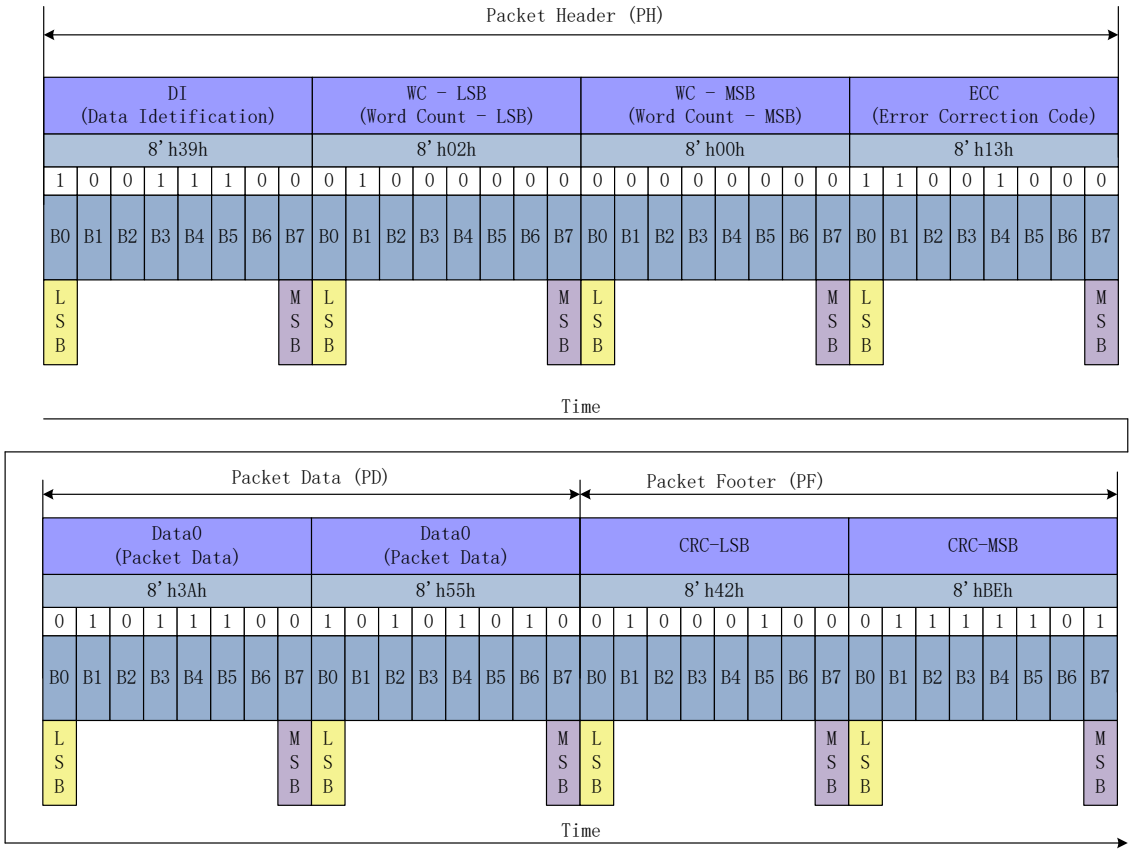
This is defined on the Long Packet (LPa) as follows.



Long Packet (LPa), when a command (1 Parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: “Interface Pixel Format (3Ah)”, Display Command Set (DCS)
  - Data 1: 55hex, Parameter of the DCS
- Packet Footer (PF)

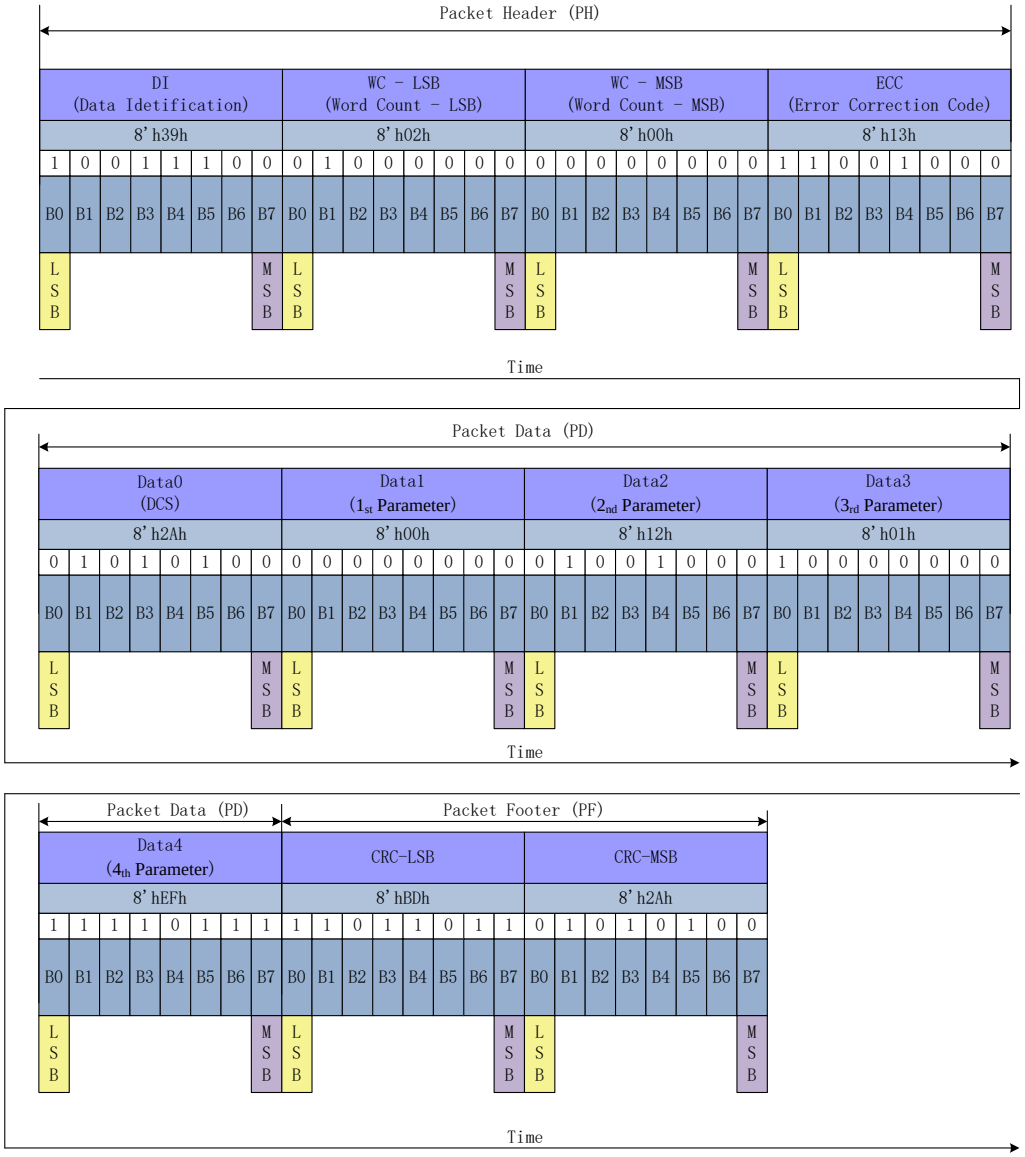
This is defined on the Long Packet (LPa) as follows.



Long Packet (LPa), when a command (4 Parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: “Column Address Set (2Ah)”, Display Command Set (DCS)
  - Data 1: 00hex, 1_{st} Parameter of the DCS, Start Column SC [15…8]
  - Data 2: 12hex, 2_{nd} Parameter of the DCS, Start Column SC [7…0]
  - Data 3: 01hex, 3_{rd} Parameter of the DCS, End Column SC [15…8]
  - Data 4: 01hex, 4_{th} Parameter of the DCS, End Column SC [7…0]
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.


Packet Header (PH)
DI
(Data Idetification)
WC - LSB
(Word Count - LSB)
WC - MSB
(Word Count - MSB)
ECC
(Error Correction Code)
8'h39h
8'h02h
8'h00h
8'h13h
Time
Packet Data (PD)
Data0
(DCS)
Data1
(1st Parameter)
Data2
(2nd Parameter)
Data3
(3rd Parameter)
8'h2Ah
8'h00h
8'h12h
8'h01h
Time
Packet Data (PD)
Packet Footer (PF)
Data4
(4th Parameter)
CRC-LSB
CRC-MSB
8'hEFh
8'hBDh
8'h2Ah
Time

3.5.1.5. Display Command Set Read, No Parameter (DCSRN-S)

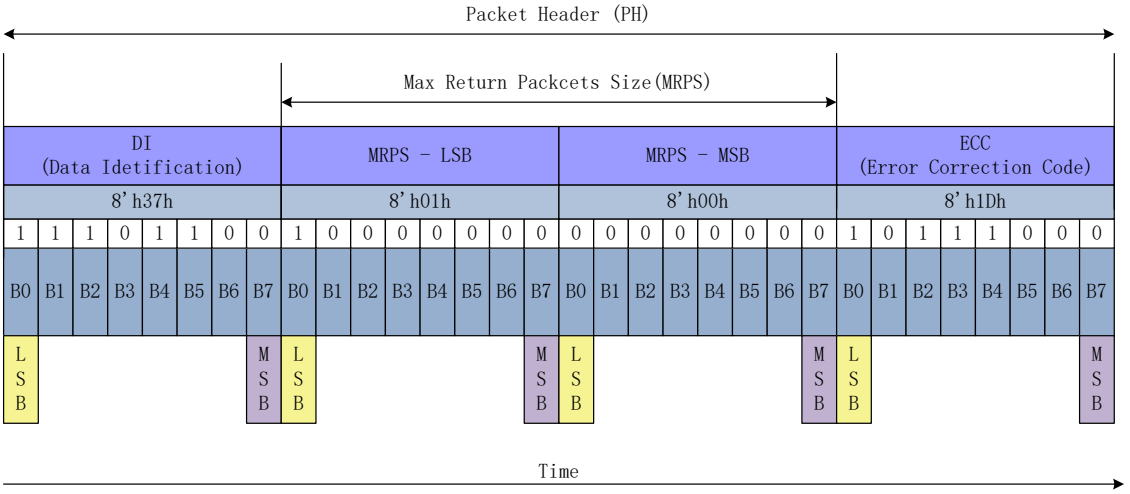
Display Command Set (DCS) Read, No Parameter" (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MCU to GC9B71. These commands are defined on a table below. The 1st parameter (Dummy Data) is not returned as it is done in MCU parallel interface. The first returned parameter is the 2nd parameter in DSI case.

Command
Read Display Power Mode (0Ah)
Read Display MADCTL (0Bh)
Read Display Pixel Format (0Ch)
Read Display Image Mode (0Dh)
Read Display Signal Mode (0Eh)
Read Display Self-Diagnostic Result (0Fh
Memory Read (2Eh)
Memory Read Continue (3Eh)
Read Display Brightness Value (52h)
Read CTRL Value Display (54h)
Read ID1 (DAh)
Read ID2 (DBh)
Read ID3 (DCh

The MCU has to define to GC9B71, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to GC9B71. This same sequence is illustrated for reference purposes below.

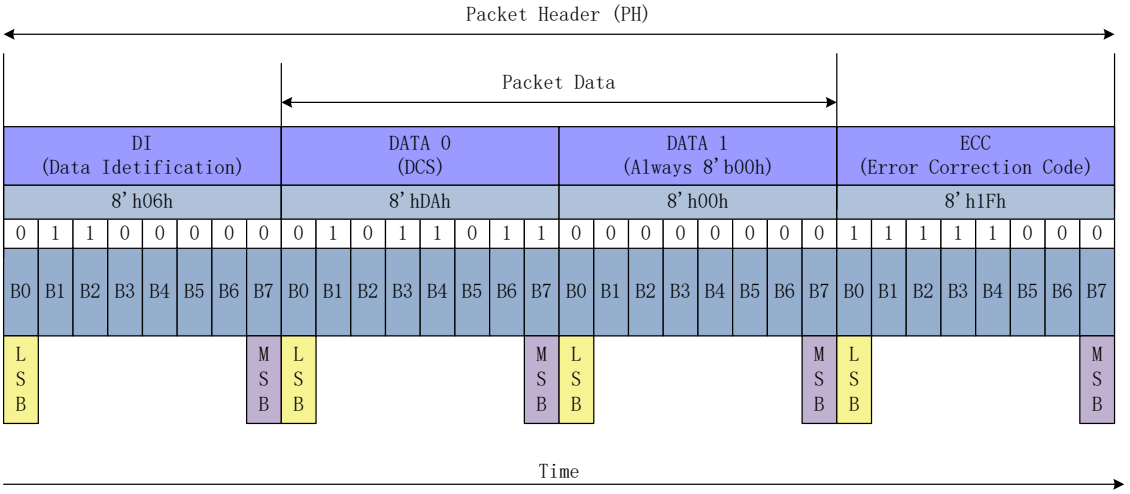
Step 1:

- The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to GC9B71 when it wants to return one byte from GC9B71
- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 0111b
- Maximum Return Packet Size (MRPS)
  - Data 0: 01hex
  - Data 1: 00hex
- Error Correction Code (ECC)



Step 2:

- The MCU wants to receive a value of the "Read ID1 (DAh)" from the display module when the MCU sends "Display Command Set (DCS) Read, No Parameter" to GC9B71
- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 0110b
- Packet Data (PD)
  - Data 0:"Read ID1 (DAh)", Display Command Set (DCS)
  - Data 1: Always 00hex
- Error Correction Code (ECC)



Step 3: GC9B71 can send 2 different informations to the MCU after Bus Turnaround (BTA)

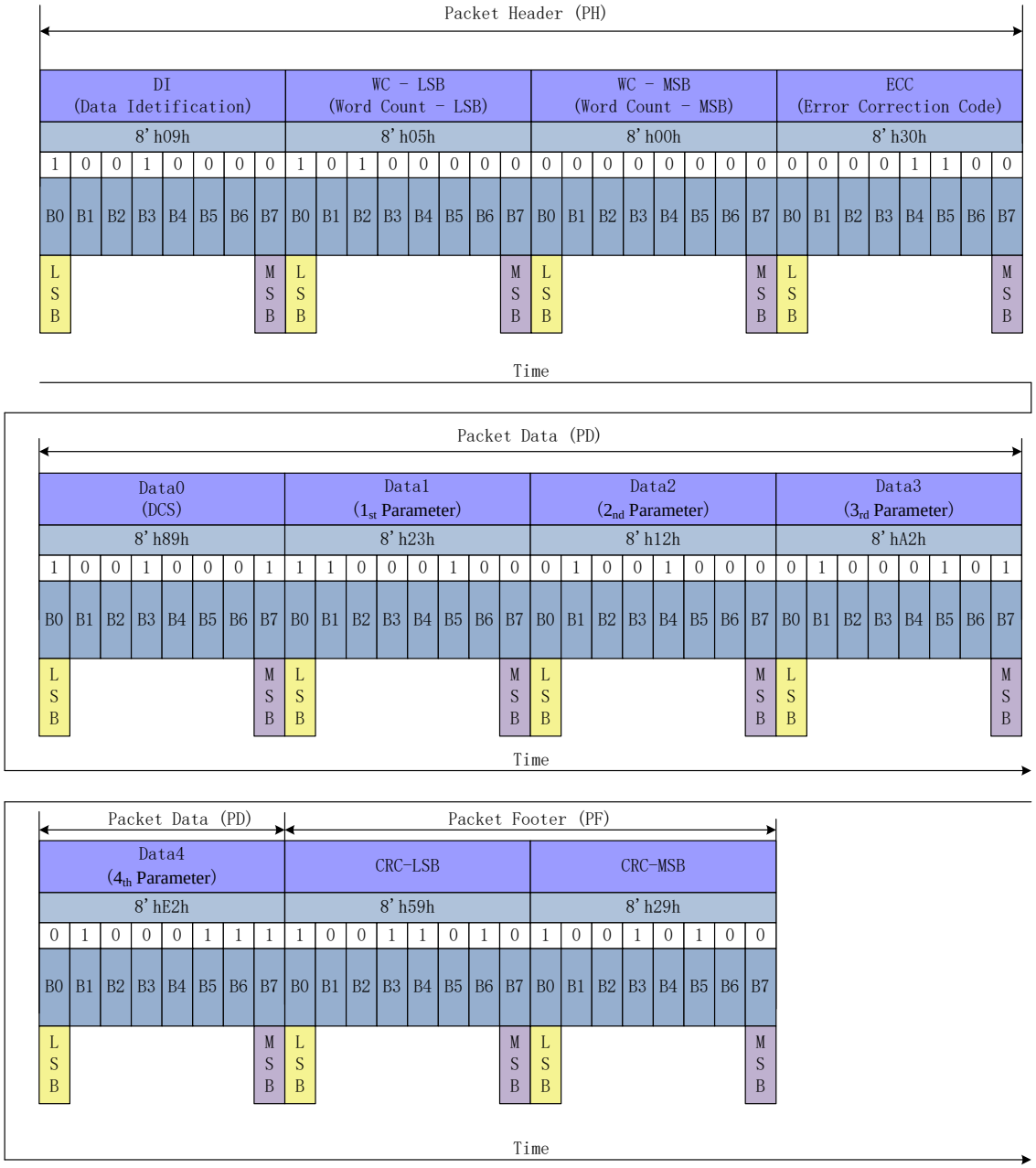
- An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command.
- Information of the received command. Short Packet (SPa) or Long Packet (LPa)

3.5.1.6. Null Packet, No Data (NP-L)

“Null Packet, No Data” (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 00 1001b), from the MCU to GC9B71. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed. GC9B71 is ignored Packet Data (PD) what the MCU is sending.
Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) were sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 1001b
- Word Count (WC)
  - Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: 89hex (Random data)
  - Data 1: 23hex (Random data)
  - Data 2: 12hex (Random data)
  - Data 3: A2hex (Random data)
  - Data 4: E2hex (Random data)
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.


Packet Header (PH)
DI
(Data Idetification)
WC - LSB
(Word Count - LSB)
WC - MSB
(Word Count - MSB)
ECC
(Error Correction Code)
8'h09h
8'h05h
8'h00h
8'h30h
1 0 0 1 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0
B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7
LSB MSB LSB MSB LSB MSB LSB MSB
Time
Packet Data (PD)
Data0
(DCS)
Data1
(1st Parameter)
Data2
(2nd Parameter)
Data3
(3rd Parameter)
8'h89h
8'h23h
8'h12h
8'hA2h
1 0 0 1 0 0 0 1 1 1 0 0 0 1 0 0 0 1 0 0 1 0 0 0 0 1 0 0 0 1 0 1
B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7
LSB MSB LSB MSB LSB MSB LSB MSB
Time
Packet Data (PD)
Packet Footer (PF)
Data4
(4th Parameter)
CRC-LSB
CRC-MSB
8'hE2h
8'h59h
8'h29h
0 1 0 0 0 1 1 1 1 0 0 1 1 0 1 0 1 0 0 1 0 1 0 0
B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7
LSB MSB LSB MSB LSB MSB
Time

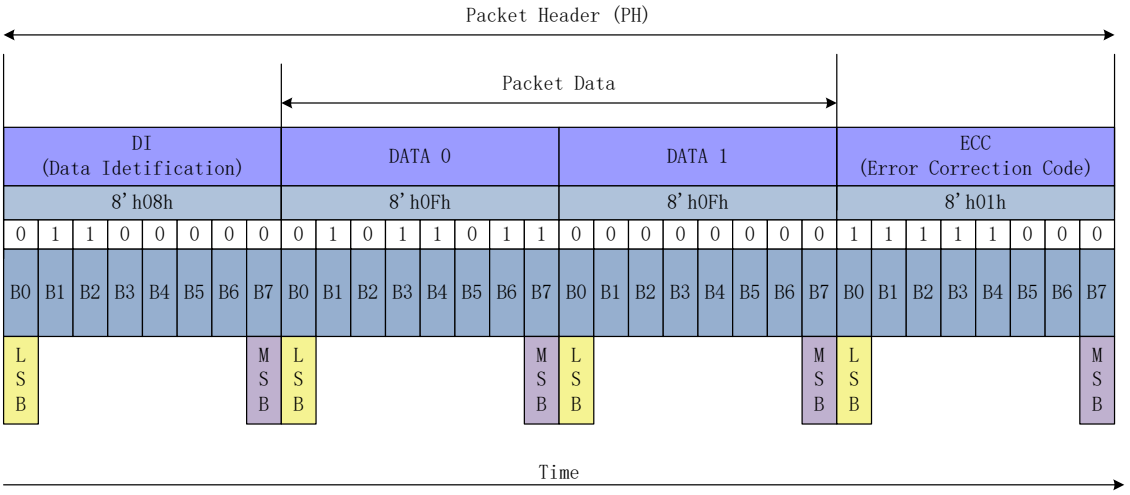
3.5.1.7. End of Transmission Packet (EoTP)

“End of Transmission Packet” (EoTP) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 1000b), from the MCU to GC9B71. The purposes of this command is terminated the high Speed Data Transmission (HSDT) mode properly when there is added this extra packet after the last payload packet before“End of Transmission” (EoT), which is an interface level functionality.
“End of Transmission Packet” (EoTP) should also be supported in the Low Power Data Transmission (LPDT) mode on GC9B71e even if this functionality has not been designed for this purposes.
The MCU can decide if it wants to use these “End of Transmission Packet” (EoTP) or not but GC9B71 has to be supporting both modes: With or Without “End of Transmission Packet” (EoTP).

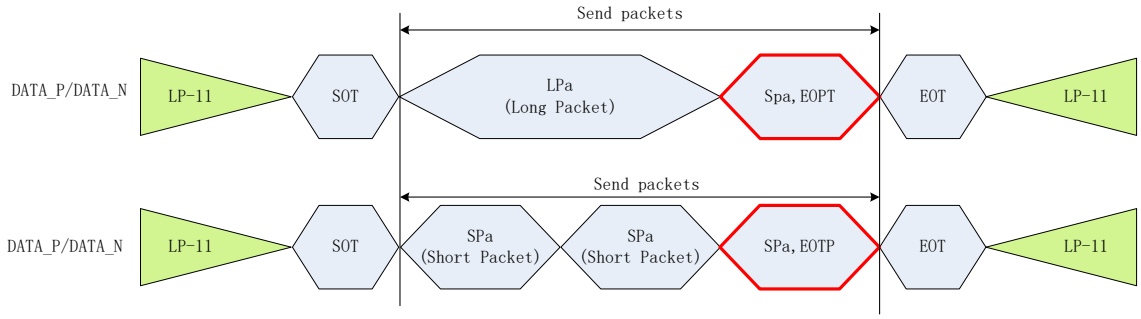
Short Packet (SPa) is using a fixed format as follows

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 1000b
- Packet Data (PD)
  - Data 0: 0Fhex
  - Data 1: 0Fhex
- Error Correction Code (ECC)
  - ECC: 01hex

This is defined on the Short Packet (SPa) as follows.



Some use cases of the “End of Transmission Packet” (EoTP) are illustrated only for reference purposes below.



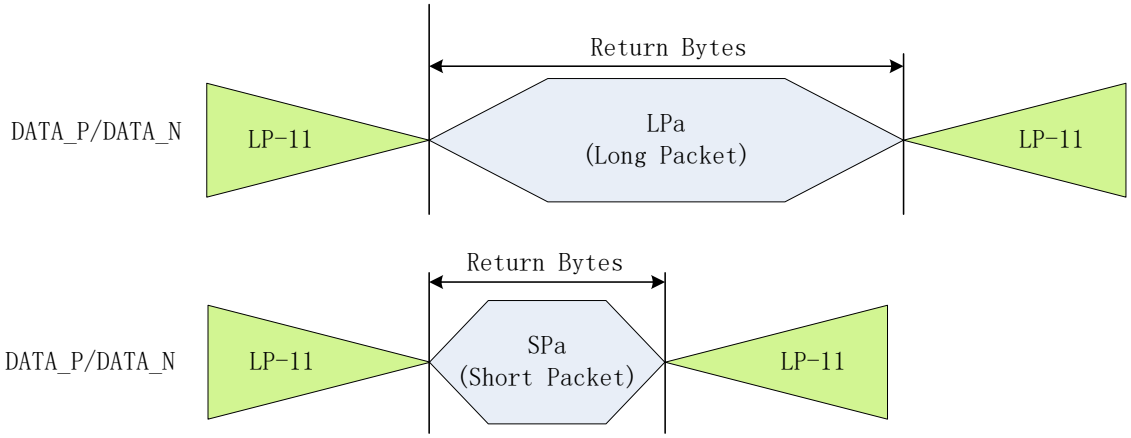
3.5.2.Packet from GC9B71 to MCU

3.5.2.1.Used Packet Types

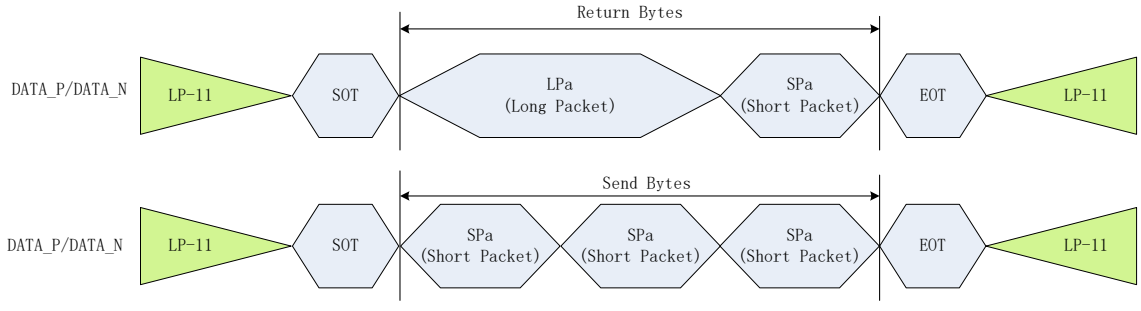
GC9B71 is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from GC9B71. This information can be a response of the Display Command Set (DCS) or an Acknowledge with Error Report (AwER). The used packet type is defined on Data Type (DT).

It is not possible that GC9B71 is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent in one packet.

The return bytes on a single packet are illustrated for reference purposes below.



The return bytes on several packets are illustrated for reference purposes below.



3.5.2.2.Acknowledge with Error Report

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0010b), from GC9B71 to the MCU.
The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to '1', as they are defined on the following table.

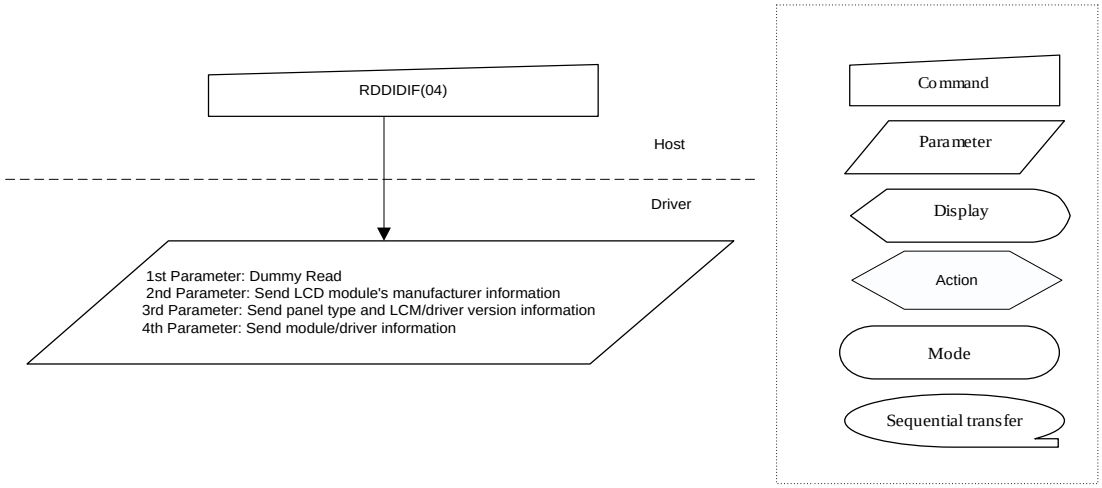
Bit	The Description of Acknowledge Error Report (AwER)	
	Short Packet	Long Packet
0	SoT Error	SoT Error
1	SoT Sync Error	SoT Sync Error
2	EoT Sync Error	EoT Sync Error
3	Escape Mode Entry Command Error	Escape Mode Entry Command Error
4	Low-Power Transmit Error	Low-Power Transmit Error
5	Any Protocol Timer-Out	Any Protocol Timer-Out
6	False Control Error	False Control Error
7	Contention is Detected on the Display Module	Contention is Detected on the Display Module
8	ECC Error, Single-Bit (Detected and Corrected)	ECC Error, Single-Bit (Detected and Corrected)
9	ECC Error, Multi-Bit (Detected, Not Corrected)	ECC Error, Multi-Bit (Detected, Not Corrected)
10	Reserved, Set to '0' internally	Checksum Error
11	DSI Data Type (DT), Not Recognized	DSI Data Type (DT), Not Recognized
12	DSI Virtual Channel (VC) ID Invalid	DSI Virtual Channel (VC) ID Invalid
13	DSI Protocol Violation	DSI Protocol Violation
14	Reserved, Set to '0' internally	Reserved, Set to '0' internally
15	Reserved, Set to '0' internally	Reserved, Set to '0' internally

These errors are included from all packages what has been received from the MCU to GC9B71, before Bus Turnaround (BTA). GC9B71 ignores the received packet which includes error or errors.

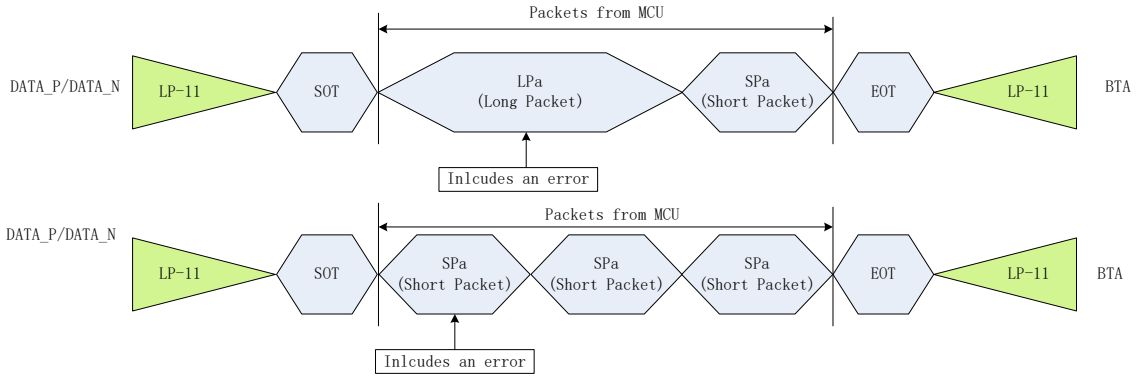
Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 0010b
- Packet Data (PD)
  - Bit 8: ECC Error, single-bit (detected and corrected)
  - AwER: 0100h
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



It is possible that GC9B71 has received several packets, which have included errors, from the MCU before the MCU is doing Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.

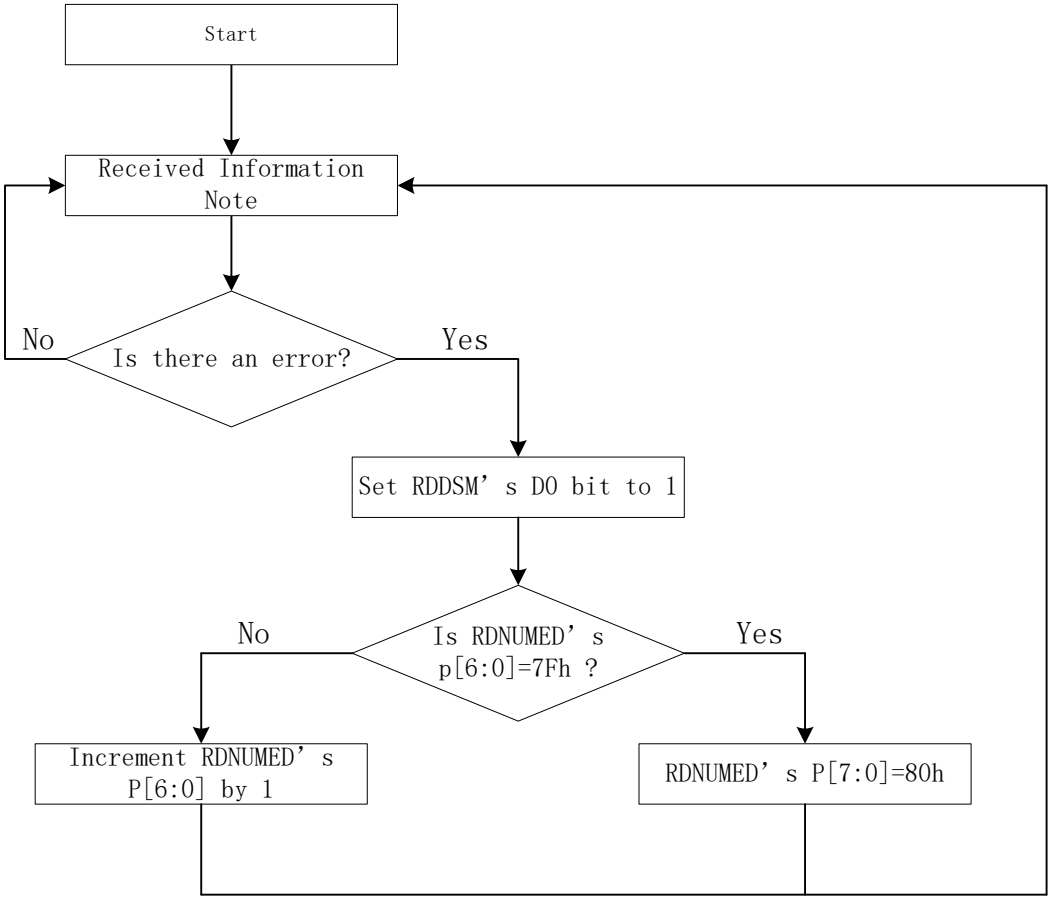


Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands.

The bit D0 of the “Read Display Signal Mode (0Eh)” command has been set to ‘1’ if a received packet includes an error.

The numbers of the packets, which are including an error, are calculated on the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the “Read Display Signal Mode (0Eh)” command to ‘0’ after the MCU has read the RDNUMED register from GC9B71.

The functionality of the RDNUMED register is illustrated for reference purposes below.



Note: This information can Interface or Packet Level Communication but it is always from the MCU to GC9B71 in this case.

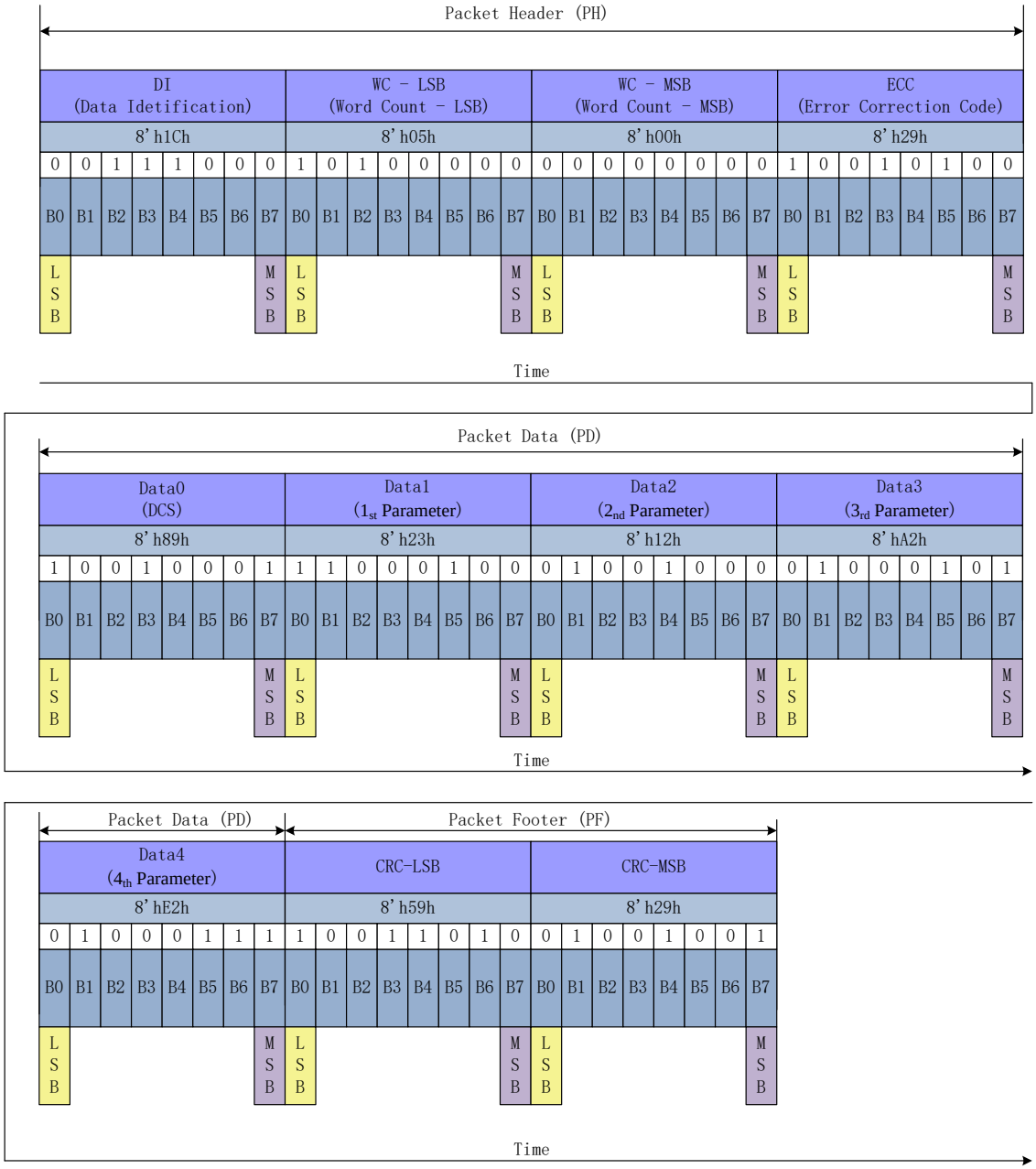
3.5.2.3.DCS Read Long Response (DCSRR-L)

“DCS Read Long Response” (DCSRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1100b), from GC9B71 to the MCU.
“DCS Read Long Response” (DCSRR-L) is used when GC9B71 wants to response a DCS Read command, which the MCU has sent to GC9B71.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
- Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 01 1100b
- Word Count (WC)
  - Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: 89hex
  - Data 1: 23hex
  - Data 2: 12hex
  - Data 3: A2hex
  - Data 4: E2hex
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.


Packet Header (PH)
DI
(Data Idetification)
WC - LSB
(Word Count - LSB)
WC - MSB
(Word Count - MSB)
ECC
(Error Correction Code)
8'h1Ch
8'h05h
8'h00h
8'h29h
0 0 1 1 1 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 1 0 0
B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7
LSB MSB LSB MSB LSB MSB LSB MSB
Time
Packet Data (PD)
Data0
(DCS)
Data1
(1st Parameter)
Data2
(2nd Parameter)
Data3
(3rd Parameter)
8'h89h
8'h23h
8'h12h
8'hA2h
1 0 0 1 0 0 0 1 1 1 0 0 0 1 0 0 0 1 0 0 1 0 0 0 0 1 0 0 0 1 0 1
B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7
LSB MSB LSB MSB LSB MSB LSB MSB
Time
Packet Data (PD)
Packet Footer (PF)
Data4
(4th Parameter)
CRC-LSB
CRC-MSB
8'hE2h
8'h59h
8'h29h
0 1 0 0 0 1 1 1 1 0 0 1 1 0 1 0 0 1 0 0 1 0 0 1
B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7
LSB MSB LSB MSB LSB MSB
Time

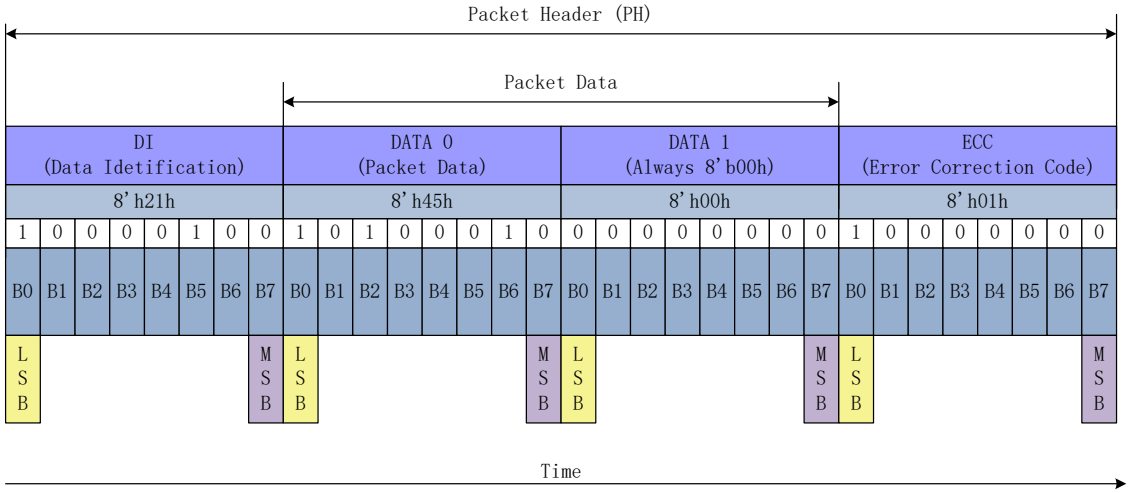
3.5.2.4.DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

“DCS Read Short Response, 1 Byte Returned” (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from GC9B71 to the MCU.
“DCS Read Short Response, 1 Byte Returned” (DCSRR1-S) is used when GC9B71 wants to response a DCS Read command, which the MCU has sent to GC9B71.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 10 0001b
- Packet Data (PD)
  - Data 0: 45hex
  - Data 1: 00hex (Always)
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows



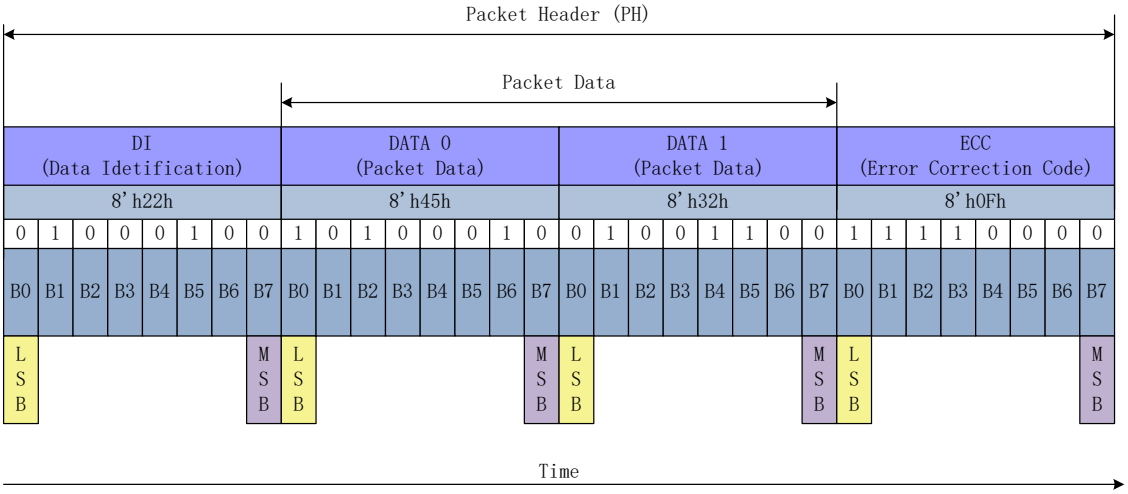
3.5.2.5. DCS Read Short Response, 2 Bytes Returned

“DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0010b), from GC9B71 to the MCU.
“DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S) is used when GC9B71 wants to response a DCS Read command, which the MCU has sent to GC9B71.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 10 0010b
- Packet Data (PD)
  - Data 0: 45hex
  - Data 1: 32hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



3.6. Communication Sequences

The communication sequences can be done on interface or packet levels between the MCU and GC9B71. This communication sequence description is for DSI data lanes (DSI-D0+/-) and it has been assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically.
Functions of the interface level communication are described on the following table.

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop State
	LPDT	Low power data transmission
	ULPS	Ultra-Low Power State
	RAR	Remote Application Reset
	TEE	Tearing Effect Event
	ACK	Acknowledge (No Error)
	BTA	Bus Turnaround
High Speed	HSDT	High speed Data Transmission

Functions of the packet level communication are described on the following table.

Interface	Mode Abbreviation	Packet Size	Interface Action Description
MCU	DCSW1-S	Short Packet	DCS Write, 1 Parameter
	DCSWN-S	Short Packet	DCS Write, No Parameter
	DCSW-L	Long Packet	DCS Write Long
	DCSRN-S	Short Packet	DCS Read, No Parameter
	SMRPS-S	Short Packet	Set Maximum Return Packet Size
	NP-L	Long Packet	Null Packet, No Data
	EoTP	Short Packet	End of Transmission Packet
GC9B71	AwER	Short Packet	Acknowledge with Error Packet
	DCSRR-L	Long Packet	DCS Read Long Response
	DCSRR1-S	Short Packet	DCS Read Short Response
	DCSRR2-S	Short Packet	DCS Read Short Response

3.6.1. DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" is defined on chapter"4.3.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" and example sequences, how this packet is used, is described on following tables.

DCS Write, 1 Parameter Sequence – Example 1						
line	MCU		Information Direction	GC9B71		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	LPDT	→	-	-	
3	-	LP-11	→	-	-	End

DCS Write, 1 Parameter Sequence – Example 2						
line	MCU		Information Direction	GC9B71		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	End

DCS Write, 1 Parameter Sequence – Example 3						
line	MCU		Information Direction	GC9B71		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	
5	-	BTA	←→	BTA	-	Interface Control Change from MCU to GC9B71
6	-	-	←	LP-11	-	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	-	-	←	ACK		No Error

9	-	-	←	LP-11	-	
10	-	BTA	←→	BTA	-	Interface Control Change from the GC9B71 to MCU
11	-	LP-11	→	-	-	End
12						
13	-	-	←	LPDT	AwER	Error Report
14	-	-	←	LP-11	-	
15	-	BTA	←→	BTA	-	
16	-	LP-11	→	-	-	End

3.6.2. DCS Write, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, No Parameter (DCSWN-S)" is defined on chapter"4.3.3.2.1.2 Display Command Set (DCS) Write, No Parameter (DCSWN-S)" and example sequences, how this packet is used, is described on following tables.

DCS Write, 0 Parameter Sequence – Example 1						
line	MCU		Information Direction	GC9B71		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	LPDT	→	-	-	
3	-	LP-11	→	-	-	End

DCS Write, 0 Parameter Sequence – Example 2						
line	MCU		Information Direction	GC9B71		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	End

DCS Write, 0 Parameter Sequence – Example 3						
line	MCU		Information Direction	GC9B71		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	
5	-	BTA	←→	BTA	-	Interface Control Change from MCU to GC9B71
6	-	-	←	LP-11	-	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	-	-	←	ACK		No Error

9	-	-	←	LP-11	-	
10	-	BTA	←→	BTA	-	Interface Control Change from the GC9B71 to MCU
11	-	LP-11	→	-	-	End
12						
13	-	-	←	LPDT	AwER	Error Report
14	-	-	←	LP-11	-	
15	-	BTA	←→	BTA	-	
16	-	LP-11	→	-	-	End

3.6.3. DCS Write, Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined on chapter “4.3.3.2.1.4 Display Command Set (DCS) Write Long (DCSW-L)” and example sequences, how this packet is used, is described on following tables.

DCS Write, Long Parameter Sequence – Example 1						
line	MCU		Information Direction	GC9B71		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-l	LPDT	→	-	-	
3	-	LP-11	→	-	-	End

DCS Write, Long Parameter Sequence – Example 2						
line	MCU		Information Direction	GC9B71		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-L	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	End

DCS Write, Long Parameter Sequence – Example 3						
line	MCU		Information Direction	GC9B71		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-L	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	
5	-	BTA	←→	BTA	-	Interface Control Change from MCU to GC9B71
6	-	-	←	LP-11	-	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	-	-	←	ACK		No Error

9	-	-	←	LP-11	-	
10	-	BTA	←→	BTA	-	Interface Control Change from the GC9B71 to MCU
11	-	LP-11	→	-	-	End
12						
13	-	-	←	LPDT	AwER	Error Report
14	-	-	←	LP-11	-	
15	-	BTA	←→	BTA	-	
16	-	LP-11	→	-	-	End

DCS Write, Long Parameter Sequence – Example 4						
line	MCU		Information Direction	GC9B71		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-L	HSDT	→	-	-	Memory Write (2Ch)
3	DCSW1-L	HSDT	→	-	-	Memory Write Continue (3Ch)
4	DCSW1-L	HSDT	→	-	-	Memory Write Continue (3Ch)
5	DCSW1-S	HSDT	→			Memory Write Continue (3Ch) with 1 Parameter
6	EoTP	HSDT	→			End of Transmission Packet
7	-	LP-11	→			End

Note: This is an example where is wanted to send image data in 4 packets.

3.6.4. DCS Read, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Read, No Parameter (DCSRN-S)" is defined on chapter "4.3.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)" and example sequences, how this packet is used, is described on following tables.

DCS Read, No Parameter Sequence – Example 1						
line	MCU		Information Direction	GC9B71		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	SMRPS-S	HSDT	→	-	-	Defined how many data byte is wanted to read : 1 byte
3	DCSW-L	HSDT	→	-	-	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	→	-	-	End of Transmission Packet
5	-	LP-11	→	-	-	
6	-	BTA	←→	BTA	-	Interface Control Change from MCU to GC9B71
7	-	-	←	LP-11	-	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is corrected by ECC →Go to Line 19
8						
9	-	-	←	ACK		Responsed 1 byte return
10	-	-	←	LP-11	-	
11	-	BTA	←→	BTA	-	Interface Control Change from the GC9B71 to MCU
12	-	LP-11	→	-	-	End
13						
14	-	-	←	LPDT	AwER	Error Report
15	-	-	←	LP-11	-	
16	-	BTA	←→	BTA	-	
17	-	LP-11	→	-	-	End
18						
19			←	LPDT	DCSRR1-S	Responsed 1 byte return
20			←	LPDT	AwER	Error Report (Error is Corrected by ECC)
21			←	LP-11	-	
22		BTA	←→	BTA	-	Interface Control Change from the GC9B71 to MCU

23		LP-11	→	-	-	End

DCS Read, No Parameter Sequence – Example 2						
line	MCU		Information Direction	GC9B71		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	SMRPS-S	HSDT	→	-	-	Defined how many data byte is wanted to read : 1 byte
3	DCSW-L	HSDT	→	-	-	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	→	-	-	End of Transmission Packet
5	-	LP-11	→	-	-	
6	-	BTA	←→	BTA	-	Interface Control Change from MCU to GC9B71
7	-	-	←	LP-11	-	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is corrected by ECC →Go to Line 19
8						
9	-	-	←	ACK		Responsed 200 byte return
10	-	-	←	LP-11	-	
11	-	BTA	←→	BTA	-	Interface Control Change from the GC9B71 to MCU
12	-	LP-11	→	-	-	End
13						
14	-	-	←	LPDT	AwER	Error Report
15	-	-	←	LP-11	-	
16	-	BTA	←→	BTA	-	
17	-	LP-11	→	-	-	End
18						
19			←	LPDT	DCSRR1-S	Responsed 200 byte return
20			←	LPDT	AwER	Error Report (Error is Corrected by ECC)
21			←	LP-11	-	
22		BTA	←→	BTA	-	Interface Control Change from the GC9B71 to MCU
23		LP-11	→	-	-	End

3.6.5. Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined on chapter “4.3.3.2.1.6 Null Packet, No Data (NP-L)” and an example sequence, how this packet is used, is described on the following table.

Null Packet, No Data Sequence – Example						
line	MCU		Information Direction	GC9B71		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	NP-L	HSDT	→	-	-	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	End

3.6.6. End of Transmission Packet

A Short Packet (SPa) of “End of Transmission Packet (EoTP)” is defined on chapter “4.3.3.2.1.7 End of Transmission Packet (EoTP)” and an example sequence, how this packet is used, is described on the following table.

End of Transmission Packet – Example						
line	MCU		Information Direction	GC9B71		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	NP-L	HSDT	→	-	-	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	End

4. Function Description

4.1. Display data GRAM mapping

The display data RAM stores display dots and consists of 360x360x18 bits. There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

Every pixel (18-bit) data in GRAM is located by a (Page, Column) address (Y, X). By specifying the arbitrary window address **SC, EC** bits and **SP, EP** bits, it is possible to access the GRAM by setting RAMWR or RAMRD commands from start positions of the window address.

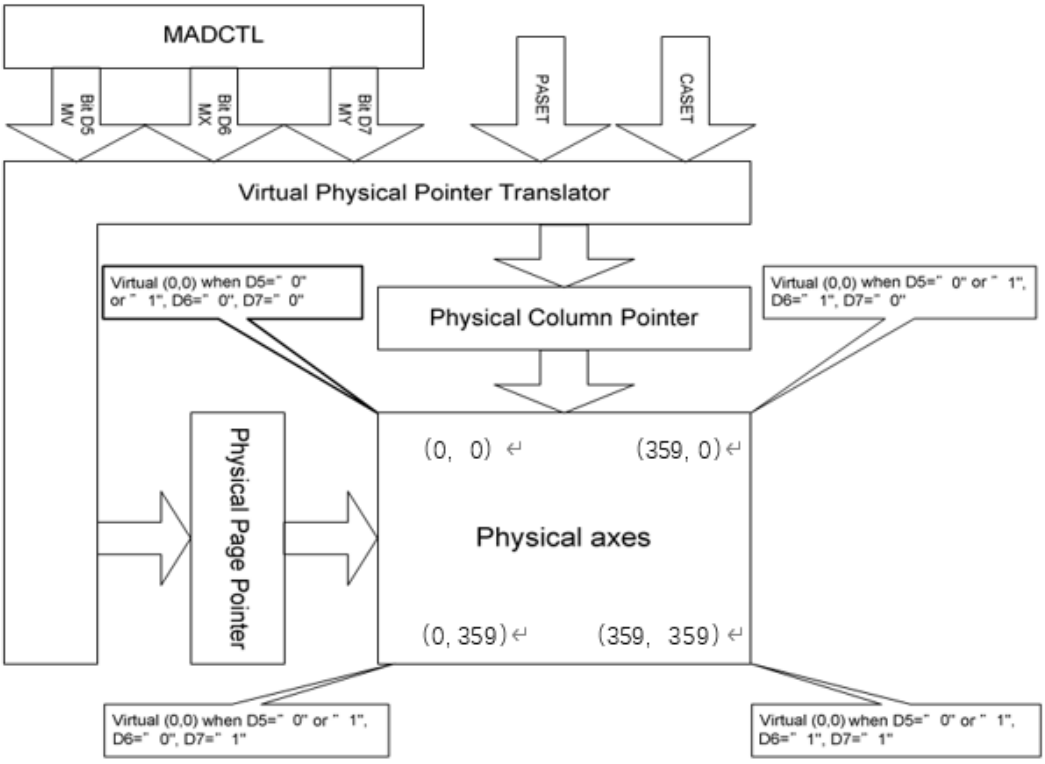
GRAM address for display panel position as shown in the following table

Table31.

(00,00)h	(00,01)h	…… …	(00, 165)h	(00, 166)h	(00,167)h
(01,00)h	(01,01)h	…… …	(01, 165)h	(01, 166)h	(01, 167)h
(02,00)h	(02,01)h	…… …	(02, 165)h	(02, 166)h	(02, 167)h
(03,00)h	(03,01)h	…… …	(03, 165)h	(03, 166)h	(03, 167)h
. . .	. . .	. . .	. . .	. . .	. . .
(165,00)h	(165,01)h	…… …	(165, 165)h	(165, 166)h	(165, 167)h
(166,00)h	(166,01)h	…… …	(166, 165)h	(165, 166)h	(166, 167)h
(167,00)h	(167,01)h	…… …	(167, 165)h	(165, 166)h	(167, 167)h

4.2. MCU to memory write/read direction

The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, Bits D5, D6, and D7 as described below.

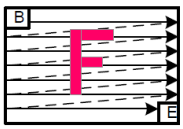
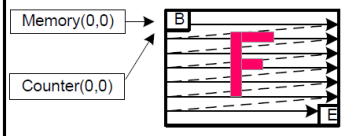
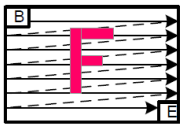
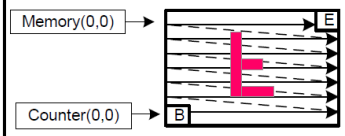
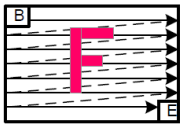
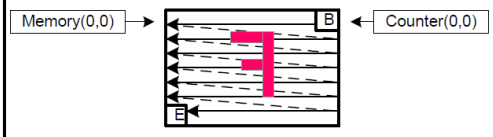
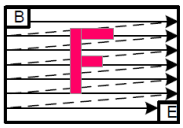
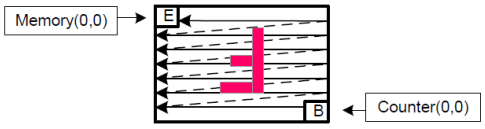
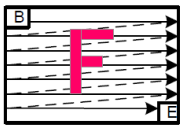
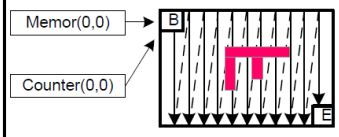
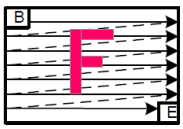
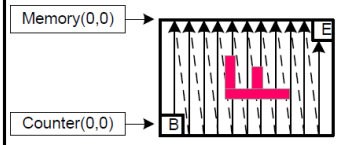
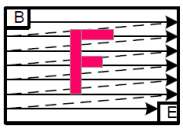
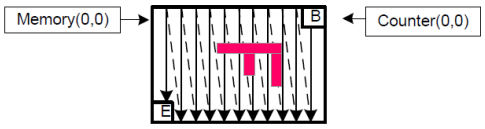
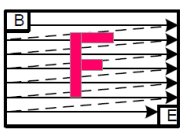
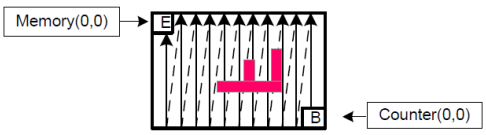


D5	D6	D7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (359-Physical Page Pointer)
0	1	0	Direct to (359-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (359-Physical Column Pointer)	Direct to (359-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (359-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (359-Physical Column Pointer)
1	1	1	Direct to (359-Physical Page Pointer)	Direct to (359-Physical Column Pointer)

Condition	Column Counter	Page counter
When RAMWR/RAMRD command is accepted	Return to “Start column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column values is large than “End Column”	Return to “Start column”	Increment by 1
The Page counter is large than “End Page”	Return to “Start column”	Return to “Start Page”

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

Display Data Direction	MADCTR Parameter			Image in the Memory (MCU)	Image in the Driver (Frame Memory)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

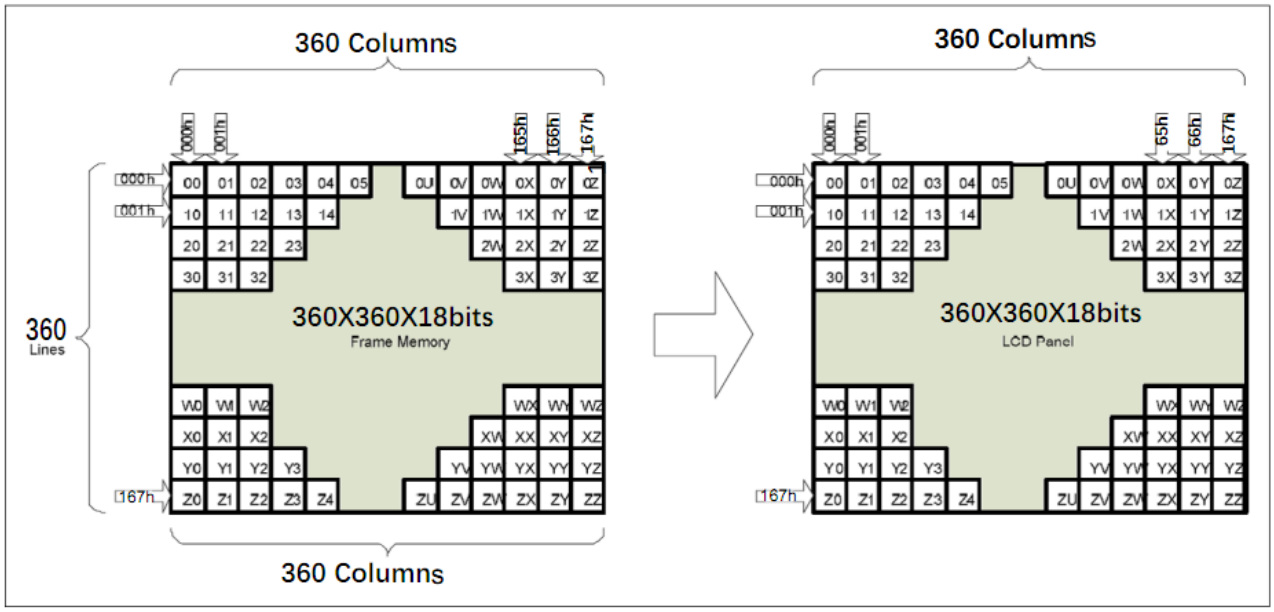
4.3. GRAM to display address mapping

By setting the **SS**, the relation between the source output channel and the GRAM address can be changed as reverse display. By setting the **GS** , the relation between the gate output channel and the GRAM address can be changed as reverse display. By setting the **BGR**, the relation between the source output channel and the <R>, <G>, <B> dot allocation can be reversed for different LCD color filter arrangement.

The following Tables show relations among the GRAM data allocation, the source output channel, and the R, G, B dot allocation.

GRAM X address and display panel position:

GC9B71 supports three kinds of display mode: one is Normal Display Mode, the other is Partial Display Mode, and Scrolling Display Mode.

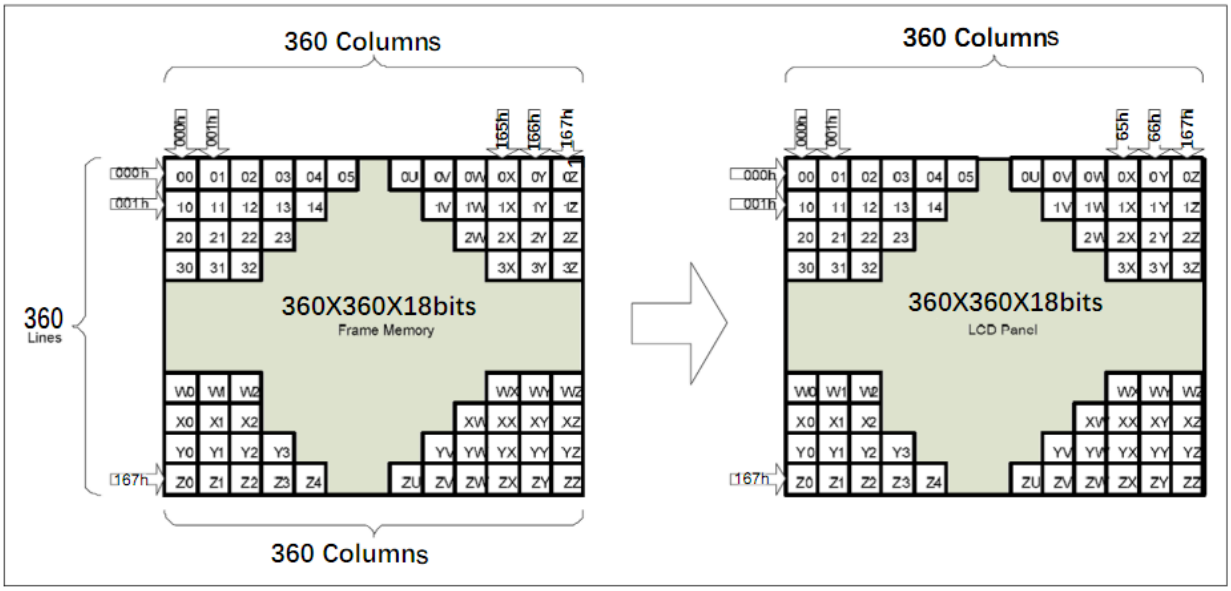


4.3.1. Normal display on or partial mode on, vertical scroll off

In this mode, content of the frame memory within an area where column pointer is 0000h to 0167h and page pointer is 0000h to 0167h is displayed.

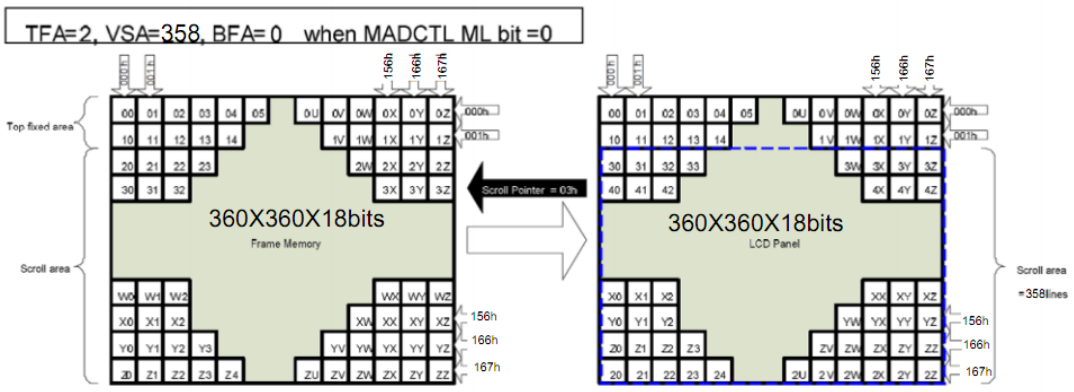
To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0)

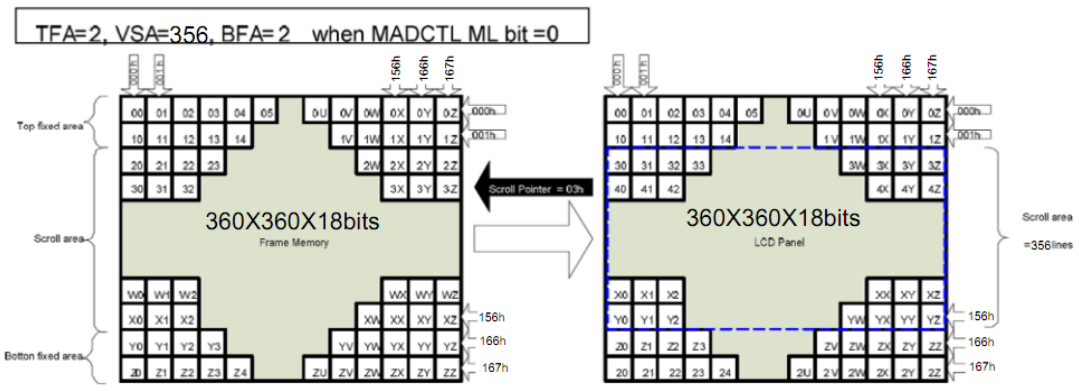
Figure66.

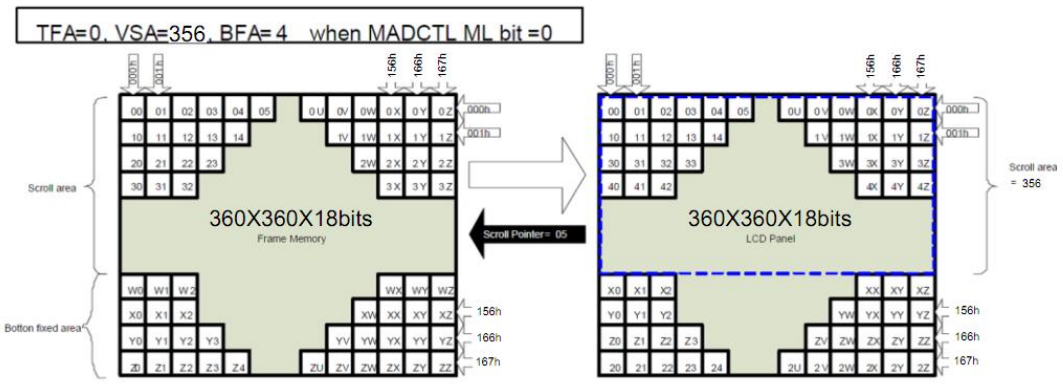


4.3.2. Vertical scroll display mode

When setting R37h, the scrolling display mode is active, and the vertical scrolling display is specified by **TFA, VSA ,BFA** bits (R33h) and **VSP** bits (R37h).







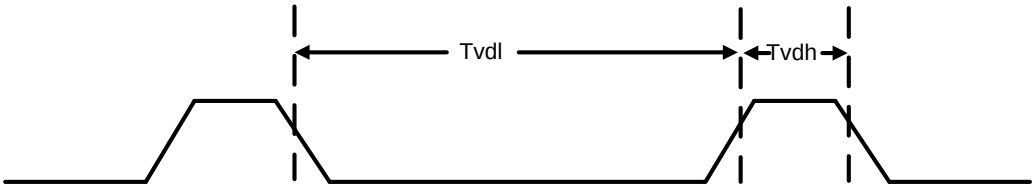
Note: When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) ≠360, Scrolling Mode is undefined.

4.4. Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

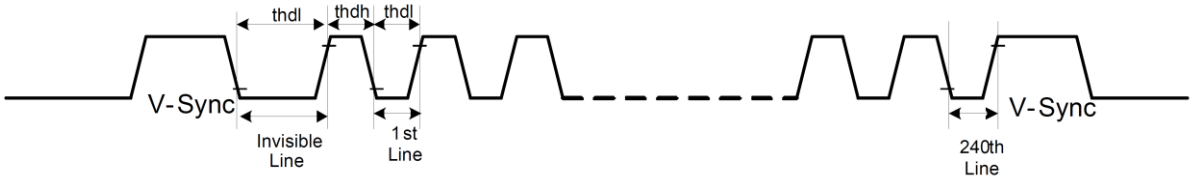
4.4.1.Tearing effect line modes

Mode 1, The Tearing Effect Output signal consists of V-Blanking Information only:
Figure79.



tVdh= The LCD display is not updated from the Frame Memory
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, The Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 360 H-sync pulses per field.
Figure80.

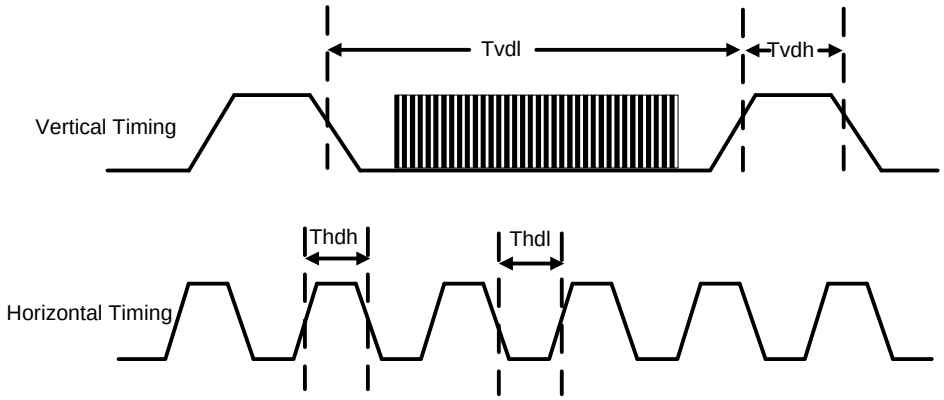


thdh= The LCD display is not updated from the Frame Memory
thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

4.4.2.Tearing effect line timing

The Tearing Effect signal is described below.

Figure81.



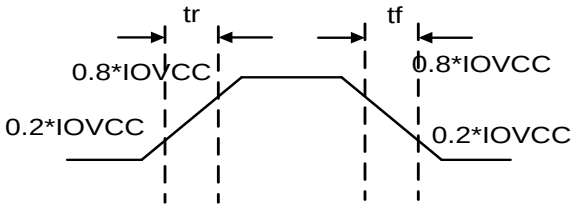
Idle Mode Off (Frame Rate = 20~65 Hz)

Table38.

Symbol	Parameter	Spec.			Description
		Min.	Max.	Unit	
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	1000	-	us	-
thdl	Horizontal Timing Low Duration	TBD	-	us	-
thdh	Horizontal Timing High Duration	TBD	500	us	-

Note: Idle Mode Off (Frame Rate = 20~65 Hz) ,The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

Figure82.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

4.5. Source driver

The GC9B71 contains a 540 channels of source driver (S1~S540) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 540 channels and generates corresponding
gray scale voltage output, which can realize a 262K colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

4.6. Gate driver

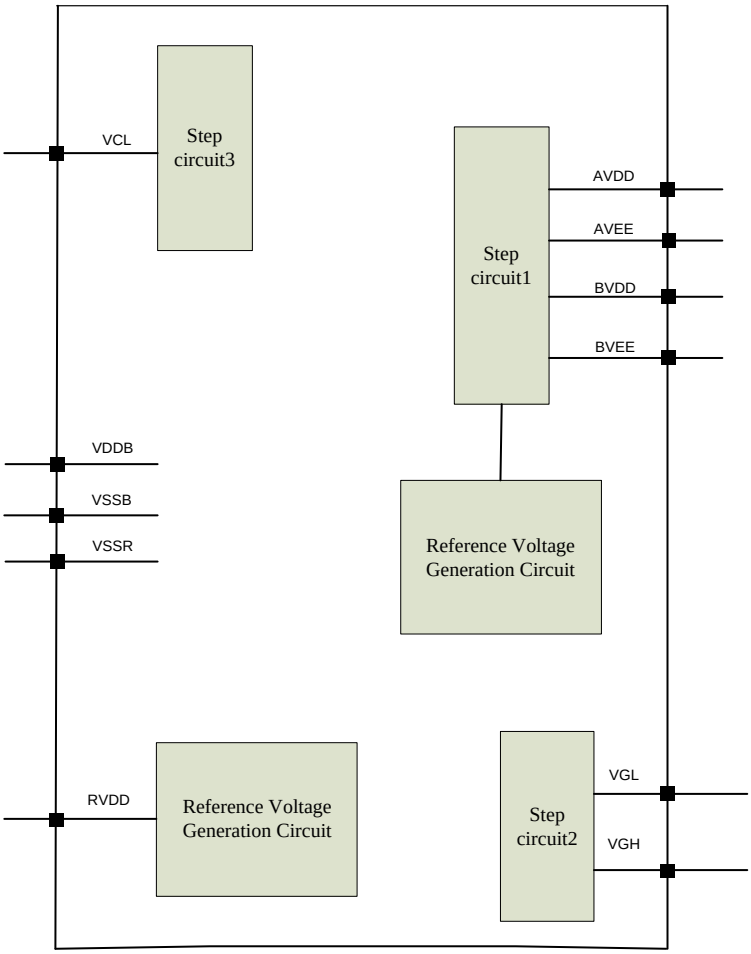
The GC9B71 contains a 32 gate channels of gate driver (G1~G32) which is used for driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

4.7. LCD power generation circuit

4.7.1. Power supply circuit

The power circuit of GC9B71 is used to generate supply voltages for LCD panel driving.

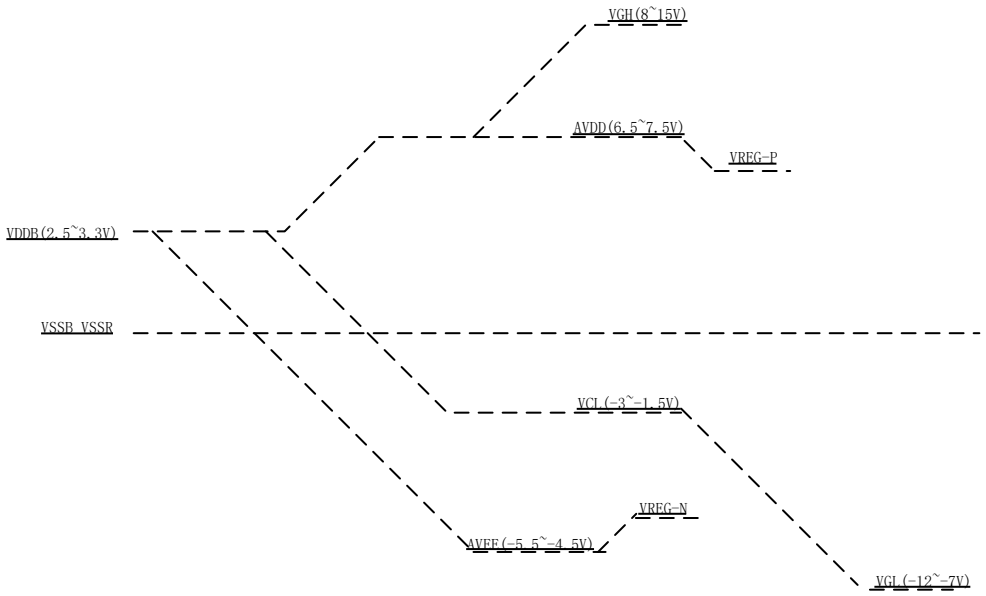
Figure83.



4.7.2.LCD power generation scheme

The boost voltage generated is shown as below.

Figure84.



LCD power generation scheme

4.8. Gamma Correction

GC9B71 incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make GC9B71 available with liquid crystal panels of various characteristics.

Figure85.

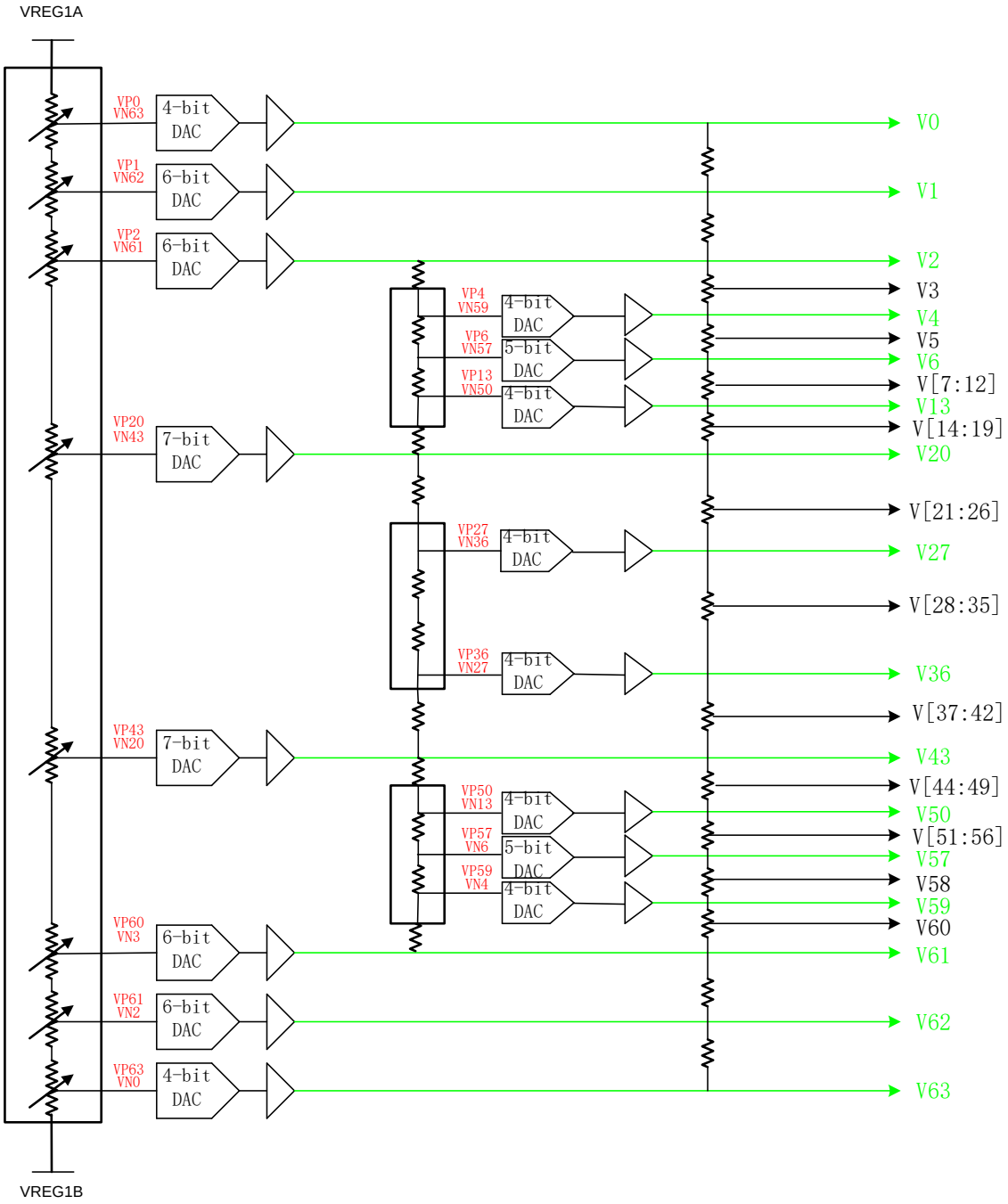
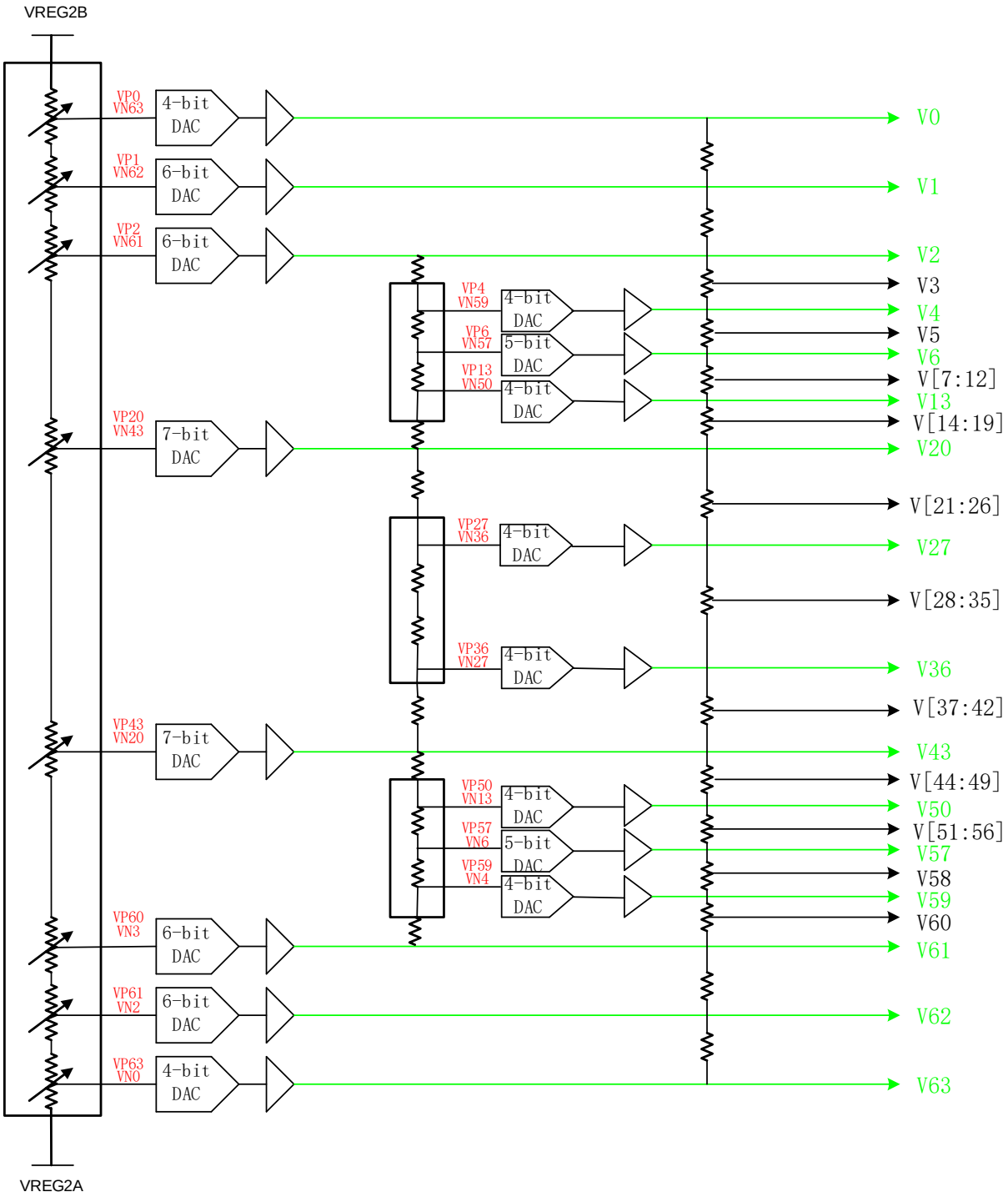
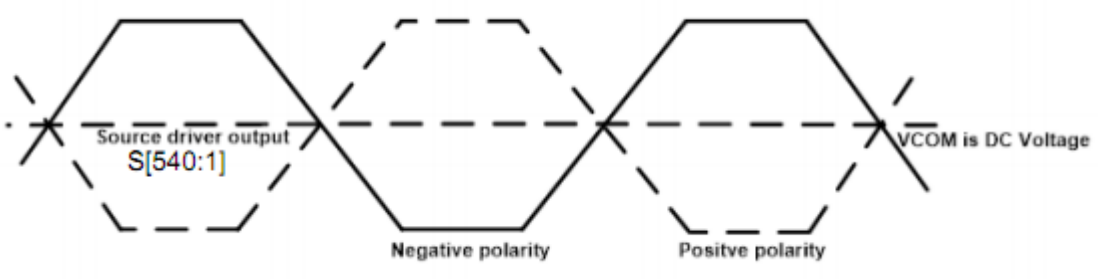


Figure86.



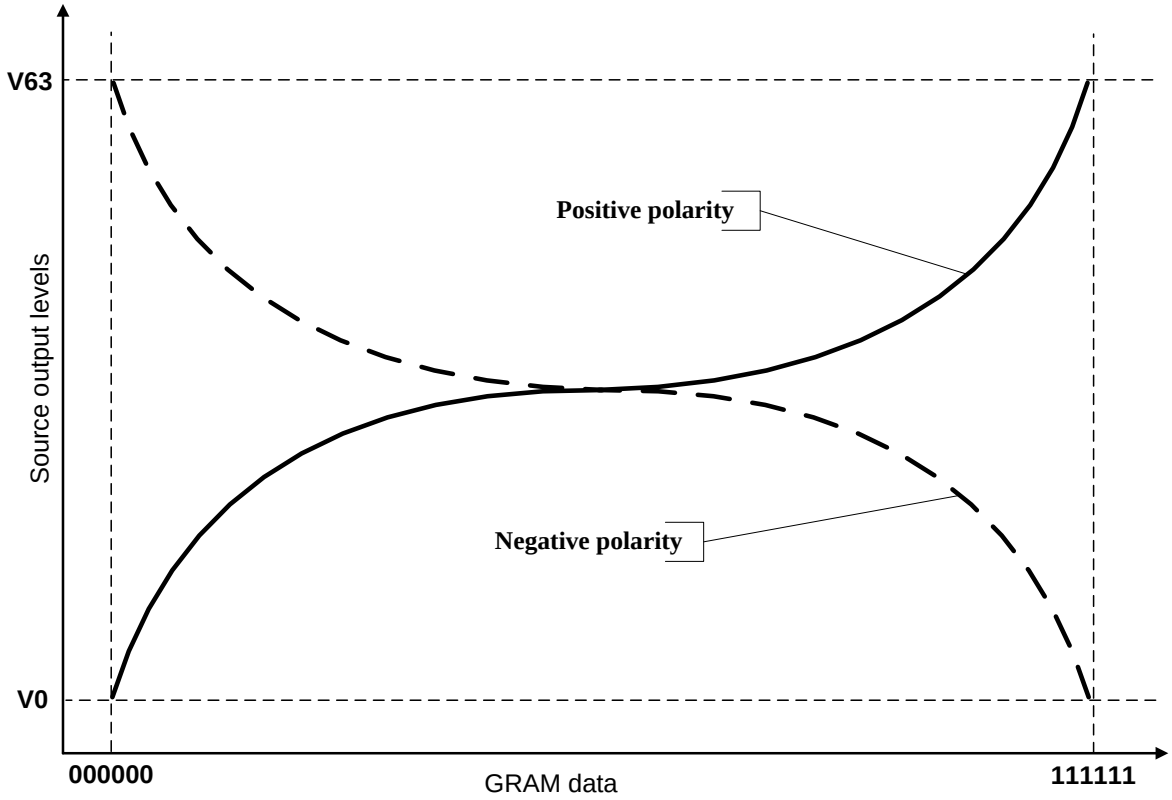
Grayscale Voltage Generation

Figure87.Dot inversion



Relationship between Source Output and VCOM

Figure88.



4.9. Power Level Definition

4.9.1. Power Levels

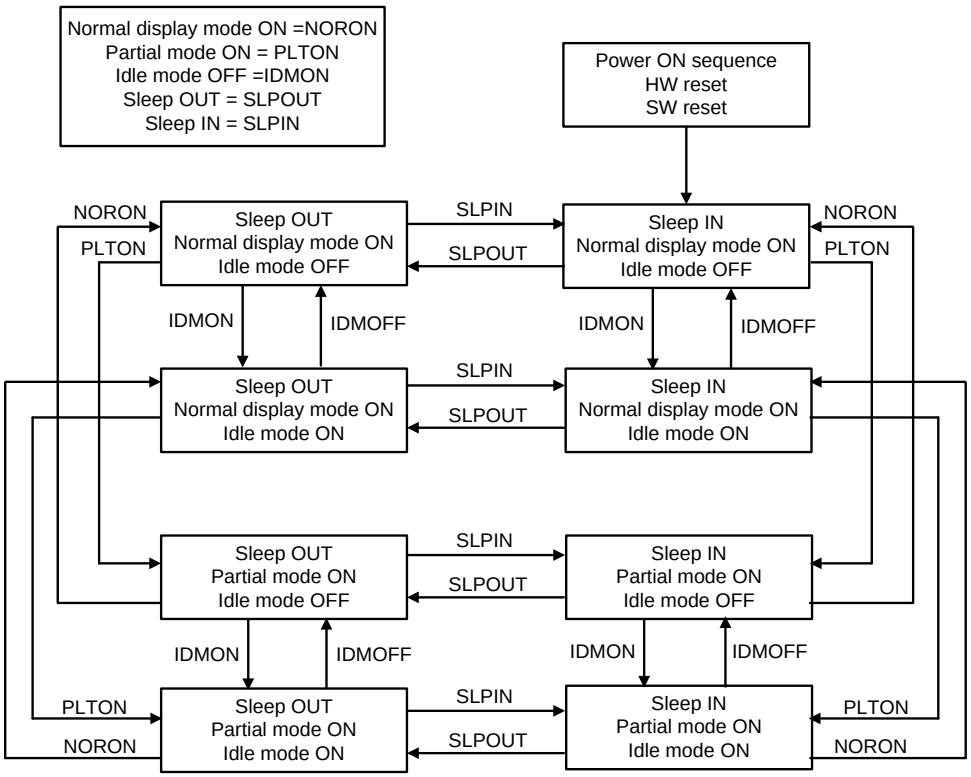
6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out.
   In this mode part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out.
   In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode.
   In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VDDB and VDDI are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

4.9.2.Power Flow Chart

Figure89.



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

4.10. Brightness control block

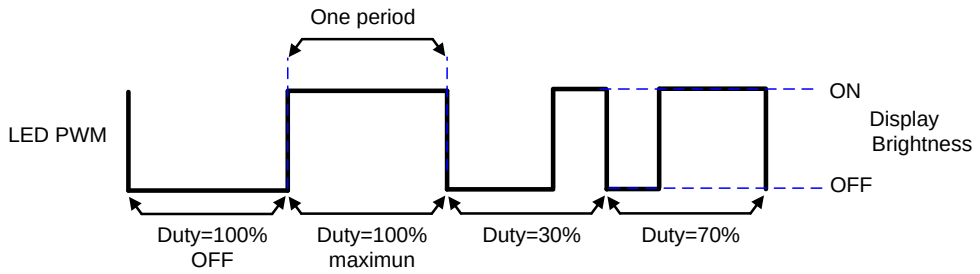
There is an external output signal from brightness block, LEDPWM to control the LED driver IC in order to control display brightness.

There are resister bits, DBV[7:0] of R51h, for display brightness of manual brightness setting. The LEDPWM duty is calculated as DBV[7:0]/255 x period (affected by OSC frequency).

For example: LEDPWM period = 3ms, and DBV[7:0] = '200DEC'. Then LEDPWM duty = 200 / 255=78.1%.

Correspond to the LEDPWM period = 3 ms, the high-level of LEDPWM (high effective) = 2.344ms, and the low-level of LEDPWM = 0.656ms.

Figure90.



LEDPWM output duty

4.11. Input/output pin state

4.11.1. Output pins

Table40.

Output or Bi-directional pins	After Power On	After Hardware Reset
DB7 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)
TE	Low	Low
BC	Low	Low

Characteristics of output pins

4.11.2. Input pins

Table41.

Input pins	During Power On Process	After Power On	After Hardware Reset	During Power Off Process
RESX	Input valid	Input valid	Input valid	Input valid
CSX	Input invalid	Input valid	Input valid	Input invalid

WRX	Input invalid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input invalid
D[7:0]	Input invalid	Input valid	Input valid	Input invalid
IM[2:0]	Input invalid	Input valid	Input valid	Input invalid

Characteristics of input pins

5. Command

5.1. Command List

Regulative Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Read Display Identification Information 2	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID_1[7:0]								00
	1	↑	1	XX	ID_2[7:0]								9B
	1	↑	1	XX	ID_3[7:0]								71
Read Display Status	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D[31:25]							X	00
	1	↑	1	XX	X	D[22:20]			D[19:16]				61
	1	↑	1	XX	X	X	X	X	X	D[10:8]			00
	1	↑	1	XX	D[7:5]			X	X	X	X	X	00
Enter Sleep Mode	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Sleep OUT	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Partial Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	0	12h
Normal Display Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	1	13h
Display Inversion OFF	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Display Inversion ON	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Display OFF	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Display ON	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Column Address Set	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
	1	1	↑	XX	SC[15:8]								00
	1	1	↑	XX	SC[7:0]								00
	1	1	↑	XX	EC[15:8]								01
	1	1	↑	XX	EC[7:0]								67h
Page Address Set	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
	1	1	↑	XX	SP[15:8]								00
	1	1	↑	XX	SP[7:0]								00
	1	1	↑	XX	EP[15:8]								01h

	1	1	↑	XX	EP[7:0]								67h
Memory Write	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
	1	1	↑	D[17:0]									XX
Partial Area	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
	1	1	↑	XX	SR[15:8]								00
	1	1	↑	XX	SR[7:0]								00
	1	1	↑	XX	ER[15:8]								01
	1	1	↑	XX	ER[7:0]								67
Vertical Scrolling Definition	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
	1	1	↑	XX	TFA[15:8]								00
	1	1	↑	XX	TFA[7:0]								00
	1	1	↑	XX	VSA[15:8]								01
	1	1	↑	XX	VSA[7:0]								67
Tearing Effect Line OFF	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
Tearing Effect Line ON	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
	1	1	↑	XX	X	X	X	X	X	X	X	M	00
Memory Access Control	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	X	X	00
Vertical Scrolling Start Address	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
	1	1	↑	XX	VSP[15:8]								00
	1	1	↑	XX	VSP[7:0]								00
Idle Mode OFF	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Idle Mode ON	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Pixel Format Set	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
	1	1	↑	XX	X	1	1	0	X	DBI[2:0]			66
Write Memory Continue	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
	1	1	↑	D[17:0]									XX
Set Tear Scanline	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
	1	1	↑	XX	X	X	X	X	X	X	X	STS[8]	00
	1	1	↑	XX	STS[7:0]								00
Get Scanline	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	X	X	GTS [8]	00
	1	↑	1	XX	GTS[7:0]								00
Write Display Brightness	0	1	↑	XX	0	1	0	1	0	0	0	1	51h
	1	↑	1	XX	DBV[7:0]								00
Write CTRL Display	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
	1	1	↑	XX	X	X	BCTRL	X	DD	BL	X	X	00
Read ID1	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh

	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								00
Read ID2	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								9B
Read ID3	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								71

Extended Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Display Function Control	0	1	1	XX	1	0	1	1	0	1	1	0	B6
	1	1	1	XX	X	X	X	X	X	X	X	X	00
	1	1	1	XX	X	GS	SS	X	X	X	X	0	00
TE Control	0	1	↑	XX	1	0	1	1	1	0	1	0	B4h
	1	1	↑	XX	te_width[7:0]								00
	1	1	↑	XX	X	X	X	X	X	X	X	te_pol	00

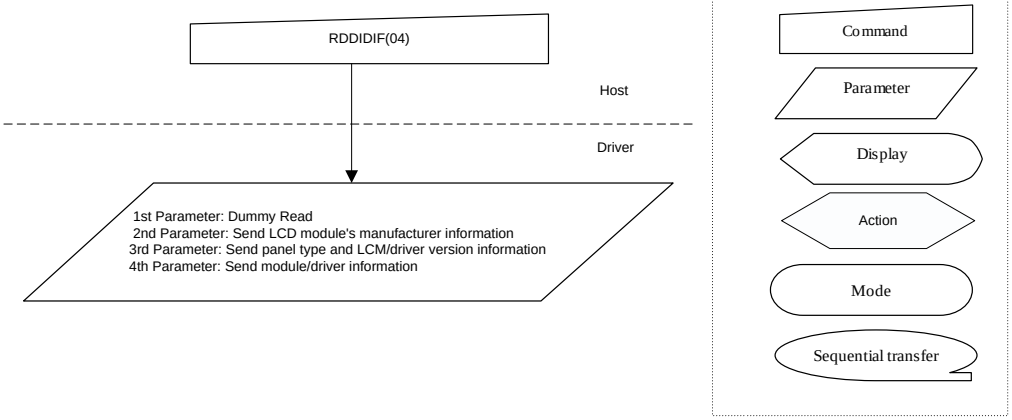
Inter Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Power Criterion Control	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h
	1	1	↑	XX	0	0	0	0	0	0	vcire	0	00
Vreg1a voltage Control	0	1	↑	XX	1	1	0	0	0	0	1	1	C3h
	1	1	↑	XX	0	vreg1_vbp_d[6:0]							3C
Vreg1b voltage Control	0	1	↑	XX	1	1	0	0	0	1	0	0	C4h
	1	1	↑	XX	0	vreg1_vbn_d[6:0]							3C
Vreg2a voltage Control	0	1	↑	XX	1	1	0	0	1	0	0	1	C9h
	1	1	↑	XX	0	0	vrh[5:0]						28
Inversion	0	1	↑	XX	1	1	1	0	1	1	0	0	ECh
	1	1	↑	XX	0	DINV[2:0]			0	0	0	0	77
	1	1	↑	XX	RTN2[7:0]								40
SPI 2data control	0	1	↑	XX	1	1	1	0	1	0	0	1	B1h
	1	1	↑	XX				DTR_EN	2data_en	2data_mdt			00
Inner register enable 1	0	1	↑	XX	1	1	1	1	1	1	1	0	FEh
Inner register enable 2	0	1	↑	XX	1	1	1	0	1	1	1	1	EFh
SET_GAMMA1	0	1	↑	XX	1	1	1	1	0	0	0	0	F0h
	1	1	↑	XX	dig2gam_dig2j0_n[		dig2gam_vr1_n[5:0]						80

					1:0]									
	1	1	↑	XX	dig2gam_dig2j1_n[1:0]		dig2gam_vr2_n[5:0]							03
	1	1	↑	XX	0	0	0	dig2gam_vr4_n[4:0]						08
	1	1	↑	XX	0	0	0	dig2gam_vr6_n[4:0]						06
	1	1	↑	XX	dig2gam_vr0_n[3:0]				dig2gam_vr13_n[3:0]					05
	1	1	↑	XX	0	dig2gam_vr20_n[6:0]								2B
SET_GAMMA2	0	1	↑	XX	1	1	1	1	0	0	0	1		F1h
	1	1	↑	XX	0	dig2gam_vr43_n[6:0]								41
	1	1	↑	XX	dig2gam_vr27_n[2:0]			dig2gam_vr57_n[4:0]						97
	1	1	↑	XX	dig2gam_vr36_n[2:0]			dig2gam_vr59_n[4:0]						98
	1	1	↑	XX	0	0	dig2gam_vr61_n[5:0]							13
	1	1	↑	XX	0	0	dig2gam_vr62_n[5:0]							17
	1	1	↑	XX	dig2gam_vr50_n[3:0]				dig2gam_vr63_n[3:0]					CD
SET_GAMMA3	0	1	↑	XX	1	1	1	1	0	0	1	0		F2h
	1	1	↑	XX	dig2gam_dig2j0_p[1:0]		dig2gam_vr1_p[5:0]							40
	1	1	↑	XX	dig2gam_dig2j1_p[1:0]		dig2gam_vr2_p[5:0]							03
	1	1	↑	XX	0	0	0	dig2gam_vr4_p[4:0]						08
	1	1	↑	XX	0	0	0	dig2gam_vr6_p[4:0]						0B
	1	1	↑	XX	dig2gam_vr0_p[3:0]				dig2gam_vr13_p[3:0]					08
	1	1	↑	XX	0	dig2gam_vr20_p[6:0]								2E
SET_GAMMA4	0	1	↑	XX	1	1	1	1	0	0	1	1		F3h
	1	1	↑	XX	0	dig2gam_vr43_p[6:0]								3F
	1	1	↑	XX	dig2gam_vr27_p[2:0]			dig2gam_vr57_p[4:0]						98
	1	1	↑	XX	dig2gam_vr36_p[2:0]			dig2gam_vr59_p[4:0]						B4
	1	1	↑	XX	0	0	dig2gam_vr61_p[5:0]							14
	1	1	↑	XX	0	0	dig2gam_vr62_p[5:0]							18
	1	1	↑	XX	dig2gam_vr50_p[3:0]				dig2gam_vr63_p[3:0]					CD

5.2. Description of Level 1 Command

5.2.1.Read display identification information (04h)

<table>
<tr><td>04h</td><td colspan="13">Read display identification information 2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>04h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID_1[7:0]</td><td>00</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID_2[7:0]</td><td>9B</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID_3[7:0]</td><td>71</td></tr>
<tr><td>Description</td><td colspan="13">This read byte returns 24 bits display identification information.
The 1st parameter is dummy data.
The 2nd parameter (ID2_1 [7:0]): LCD module’s manufacturer ID.
The 3rd parameter (ID2_2 [7:0]): LCD module/driver version ID.
The 4th parameter (ID2_3 [7:0]): LCD module/driver ID.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>24’h009B71</td></tr><tr><td>SW Reset</td><td>24’h009B71</td></tr><tr><td>HW Reset</td><td>24’h009B71</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"></td></tr>
</table>


RDDIDIF(04)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send LCD module's manufacturer information
3rd Parameter: Send panel type and LCM/driver version information
4th Parameter: Send module/driver information
Command
Parameter
Display
Action
Mode
Sequential transfer

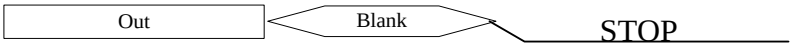
5.2.2.Read Display Status (09h)

<table>
<tr><td>09h</td><td colspan="13">Read Display Status</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>09h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">D[31:25]</td><td>X</td><td>00</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td colspan="4">D[22:20]</td><td colspan="4">D[19:16]</td><td>61</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="3">D[10:8]</td><td>00</td></tr>
<tr><td>5th Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="4">D[7:5]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th><th>Status</th></tr>
<tr><td>D31</td><td>Booster voltage status</td><td>O</td><td>Booster OFF</td></tr>
<tr><td></td><td></td><td>1</td><td>Booster ON</td></tr>
<tr><td>D30</td><td>Row address order</td><td>O</td><td>Top to Bottom (When MADCTL B7='0')</td></tr>
<tr><td></td><td></td><td>1</td><td>Bottom to Top (When MADCTL B7='1')</td></tr>
<tr><td>D29</td><td>Column address order</td><td>O</td><td>Left to Right (When MADCTL B6='0').</td></tr>
<tr><td></td><td></td><td>1</td><td>Right to Left (When MADCTL B6='1').</td></tr>
<tr><td>D28</td><td>Row/column exchange</td><td>O</td><td>Normal Mode (When MADCTL B5='0').</td></tr>
<tr><td></td><td></td><td>1</td><td>Reverse Mode (When MADCTL B5='1').</td></tr>
<tr><td>D27</td><td>Vertical refresh</td><td>O</td><td>LCD Refresh Top to BoUom (When MADCTL B4='0')</td></tr>
<tr><td></td><td></td><td>1</td><td>LCD Refresh BoUom to Top (When MADCTL B4='1').</td></tr>
<tr><td>D26</td><td>RGB/BGR order</td><td>O</td><td>RGB (When MADCTL B3='0')</td></tr>
<tr><td></td><td></td><td>1</td><td>BGR (When MADCTL B3='1')</td></tr>
<tr><td>D25</td><td>Horizontal refresh order</td><td>O</td><td>LCD Refresh Left to Right (When MADCTL B2='0')</td></tr>
<tr><td></td><td></td><td>1</td><td>LCD Refresh Right to Left (When MADCTL B2='1')</td></tr>
<tr><td>D24</td><td>Not used</td><td>O</td><td>-</td></tr>
<tr><td>D23</td><td>Not used</td><td>O</td><td>-</td></tr>
<tr><td>D22</td><td rowspan="3">Interface color pixel format definition</td><td rowspan="2">101</td><td rowspan="2">16-bit/pixel</td></tr>
<tr><td>D21</td></tr>
<tr><td>D20</td><td>110</td><td>18-bit/pixel</td></tr>
<tr><td>D19</td><td>Idle mode ON/OFF</td><td>O</td><td>Idle Mode OFF</td></tr>
<tr><td></td><td></td><td>1</td><td>Idle Mode ON</td></tr>
<tr><td>D18</td><td>Partial mode ON/OFF</td><td>O</td><td>Partial Mode OFF</td></tr>
<tr><td></td><td></td><td>1</td><td>Partial Mode ON</td></tr>
<tr><td>D17</td><td>Sleep IN/OUT</td><td>O</td><td>Sleep IN Mode</td></tr>
</table></td></tr>
</table>

				1	Sleep OUT Mode
		D16	Display normal mode ON/OFF	O	Display Normal Mode OFF.
				1	Display Normal Mode ON.
		D15	Vertical scrolling status	O	Scroll OFF
		D14	Not used	O	-
		D13	Inversion status	O	Not defined
		D12	All pixel ON	O	Not defined
		D11	All pixel OFF	O	Not defined
		D10	Display ON/OFF	O	
				1	Display is ON
		D9	Tearing effect line ON/OFF	O	Tearing Effect Line OFF
				1	Tearing Effect ON
		D5	Tearing effect line mode	0	Mode 1, V-Blanking only
				1	Mode 2, both H-Blanking and V-Blanking
		D4	Not used	O	-
		D3	Not used	O	-
		D2	Not used	O	-
		D1	Not used	O	-
		D0	Not used	O	-
Restriction					
Register Availability					

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

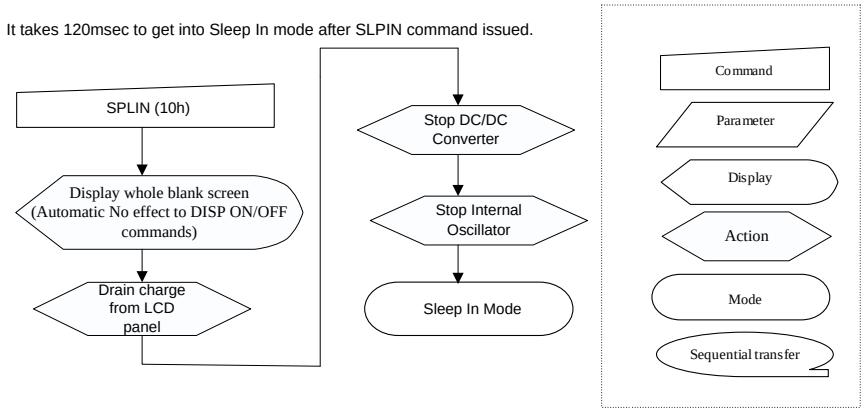
5.2.3.Enter Sleep Mode (10h)

10h	Enter Sleep Mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Parameter	No Parameter												
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped  MCU interface and memory are still working and the memory keeps its contents. X = Don't care												
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

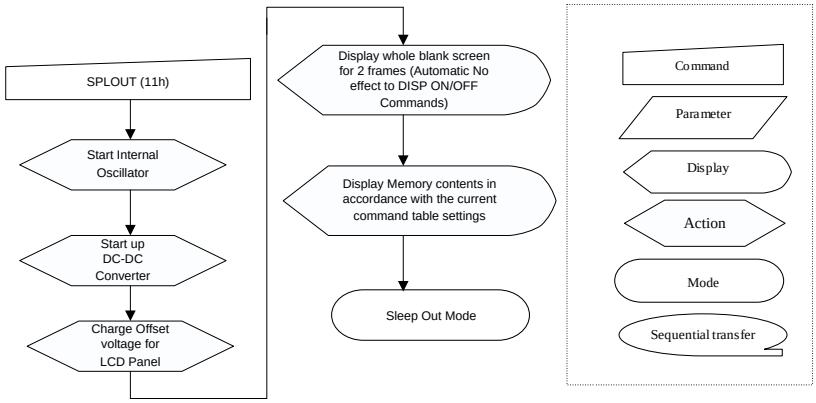
Status	Default Value
Power On Sequence	Sleep IN Mode
SW Reset	Sleep IN Mode
HW Reset	Sleep IN Mode

Flow Chart	

It takes 120msec to get into Sleep In mode after SLPIN command issued.
SPLIN (10h)
Display whole blank screen (Automatic No effect to DISP ON/OFF commands)
Drain charge from LCD panel
Stop DC/DC Converter
Stop Internal Oscillator
Sleep In Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

5.2.4.Sleep Out Mode (11h)

<table>
<tr><td>11h</td><td colspan="13">Sleep Out Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>11h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns off sleep mode.
the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits stabilize. The display module loads all display supplier’s factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr><tr><td>SW Reset</td><td>Sleep IN Mode</td></tr><tr><td>HW Reset</td><td>Sleep IN Mode</td></tr></table></td></tr>
</table>

Flow Chart	

SPLOUT (11h)
Start Internal Oscillator
Start up DC-DC Converter
Charge Offset voltage for LCD Panel
Display whole blank screen for 2 frames (Automatic No effect to DISP ON/OFF Commands)
Display Memory contents in accordance with the current command table settings
Sleep Out Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

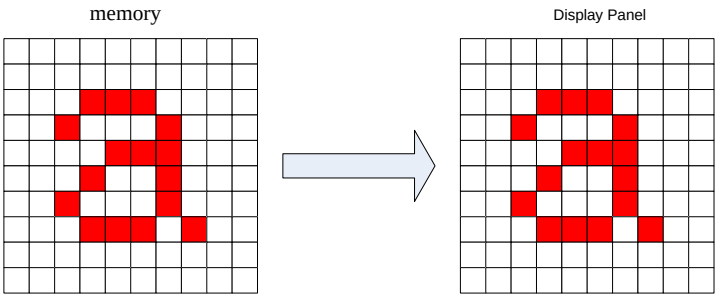
5.2.5.Partial Mode ON (12h)

<table>
<tr><td>12h</td><td colspan="13">Partial Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

5.2.6.Normal Display Mode ON (13h)

<table>
<tr><td>13h</td><td colspan="13">Normal Display Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command returns the display to normal mode.
Normal display mode on means Partial mode off.
Exit from NORON by the Partial mode On command (12h)
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

5.2.7.Display Inversion OFF (20h)

20h	Display Inversion OFF												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Parameter	No Parameter												
Description	This command is used to recover from display inversion mode. This command makes no change of the content of frame memory. This command doesn't change any other status.  X = Don't care												
Restriction	This command has no effect when module already is inversion OFF mode.												

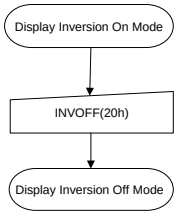
Register Availability

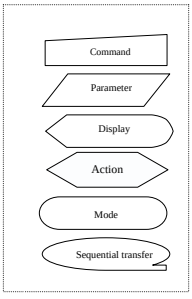
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

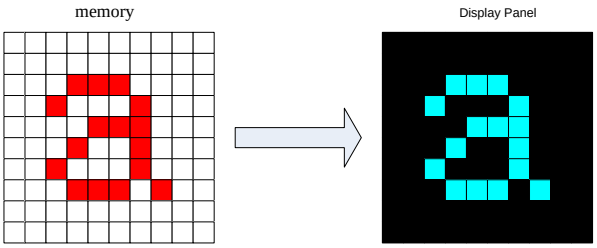
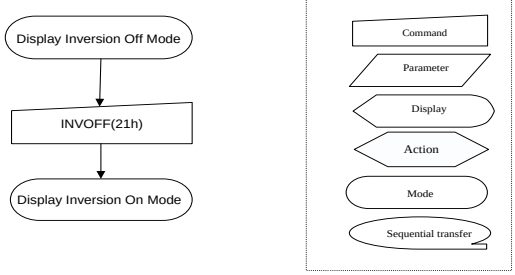
Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart

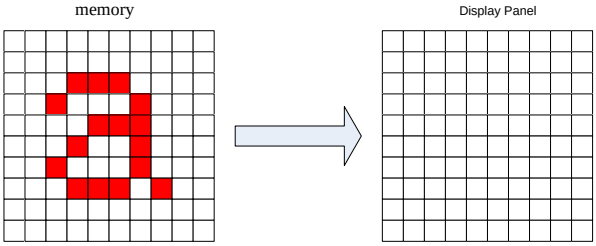


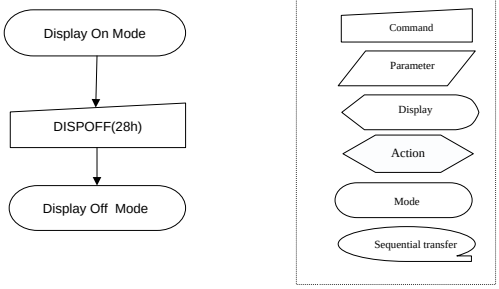


5.2.8.Display Inversion ON (21h)

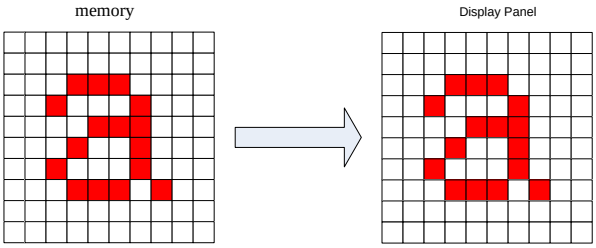
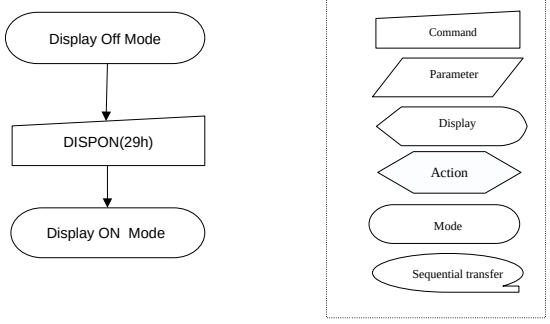
<table>
<tr><td>21h</td><td colspan="13">Display Inversion ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>21h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enter into display inversion mode.
This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display.
This command doesn’t change any other status.
To exit Display inversion mode, the Display inversion OFF command (20h) should be written..
 
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module already is inversion ON mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion OFF</td></tr><tr><td>SW Reset</td><td>Display Inversion OFF</td></tr><tr><td>HW Reset</td><td>Display Inversion OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">  </td></tr>
</table>

5.2.9.Display OFF (28h)

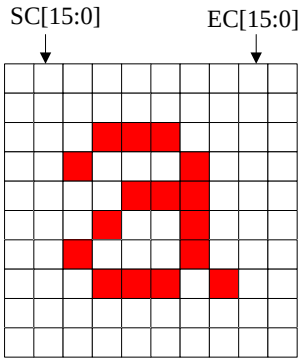
<table>
<tr><td>28h</td><td colspan="13">Display OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>28h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.
This command makes no change of contents of frame memory.
This command does not change any other status.
There will be no abnormal visible effect on the display.
 

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in display off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display OFF</td></tr><tr><td>SW Reset</td><td>Display OFF</td></tr><tr><td>HW Reset</td><td>Display OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

5.2.10. Display ON (29h)

<table>
<tr><td>29h</td><td colspan="13">Display ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>29h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.
 
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in display on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display OFF</td></tr><tr><td>SW Reset</td><td>Display OFF</td></tr><tr><td>HW Reset</td><td>Display OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">  </td></tr>
</table>

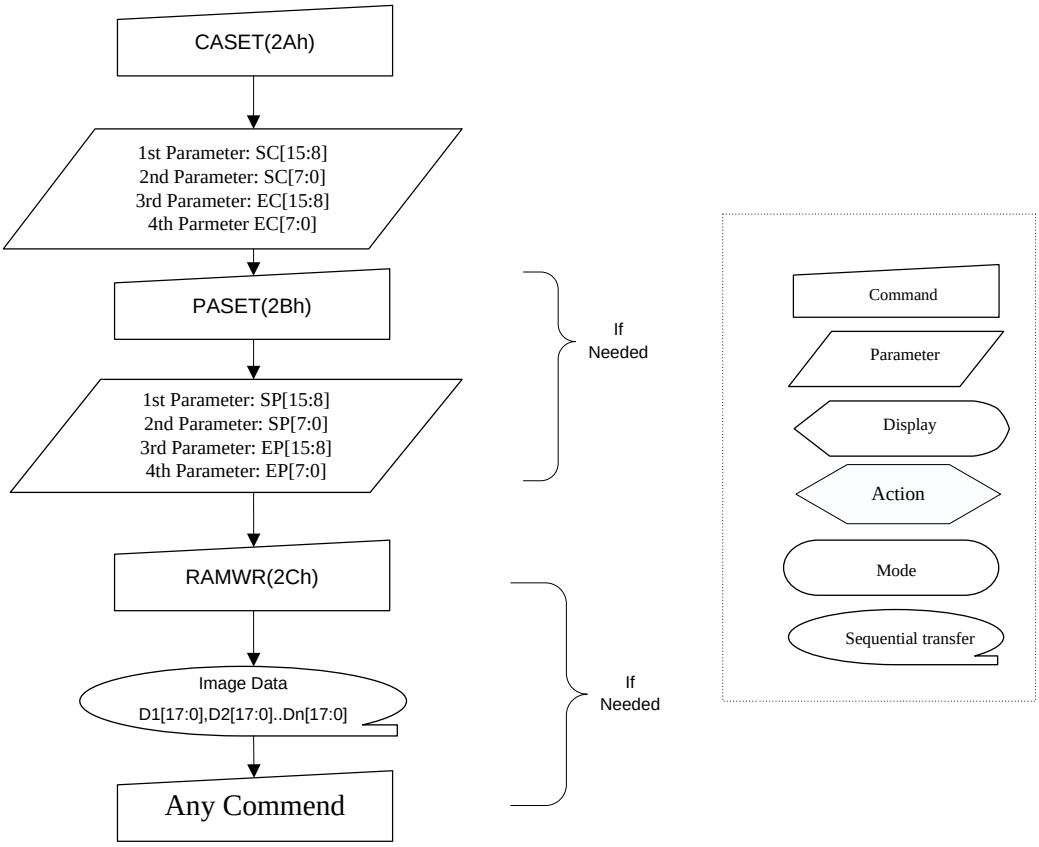
5.2.11. Column Address Set (2Ah)

<table>
<tr><td>2Ah</td><td colspan="13">Column Address Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>2Ah</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SC15</td><td>SC14</td><td>SC13</td><td>SC12</td><td>SC11</td><td>SC10</td><td>SC9</td><td>SC8</td><td rowspan="2">Note1</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SC7</td><td>SC6</td><td>SC5</td><td>SC4</td><td>SC3</td><td>SC2</td><td>SC1</td><td>SC0</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EC15</td><td>EC14</td><td>EC13</td><td>EC12</td><td>EC11</td><td>EC10</td><td>EC9</td><td>EC8</td><td rowspan="2">Note1</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EC7</td><td>EC6</td><td>EC5</td><td>EC4</td><td>EC3</td><td>EC2</td><td>EC1</td><td>EC0</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command comes. Each value
represents one column line in the Frame Memory..
 

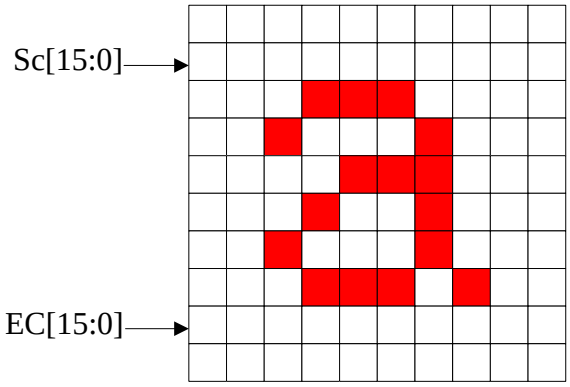
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">SC [15:0] always must be equal to or less than EC [15:0].
Note 1: When SC [15:0] or EC [15:0] is greater than 013Fh (When MADCTL’s B5 = 0) or 0167h (When MADCTL’s B5 = 1), data of out of range will be ignored</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th colspan="2">Default Value</th></tr><tr><td>Power On Sequence</td><td>SC [15:0]=0000h</td><td>EC [15:0]=0167h</td></tr><tr><td>SW Reset</td><td>SC [15:0]=0000h</td><td>If MADCTL’s B5 = 0: EC [15:0]=0167h</td></tr></table></td></tr>
</table>

			If MADCTL's B5 = 1: EC [15:0]=0167h
	HW Reset	SC [15:0]=0000h	EC [15:0]=0167h

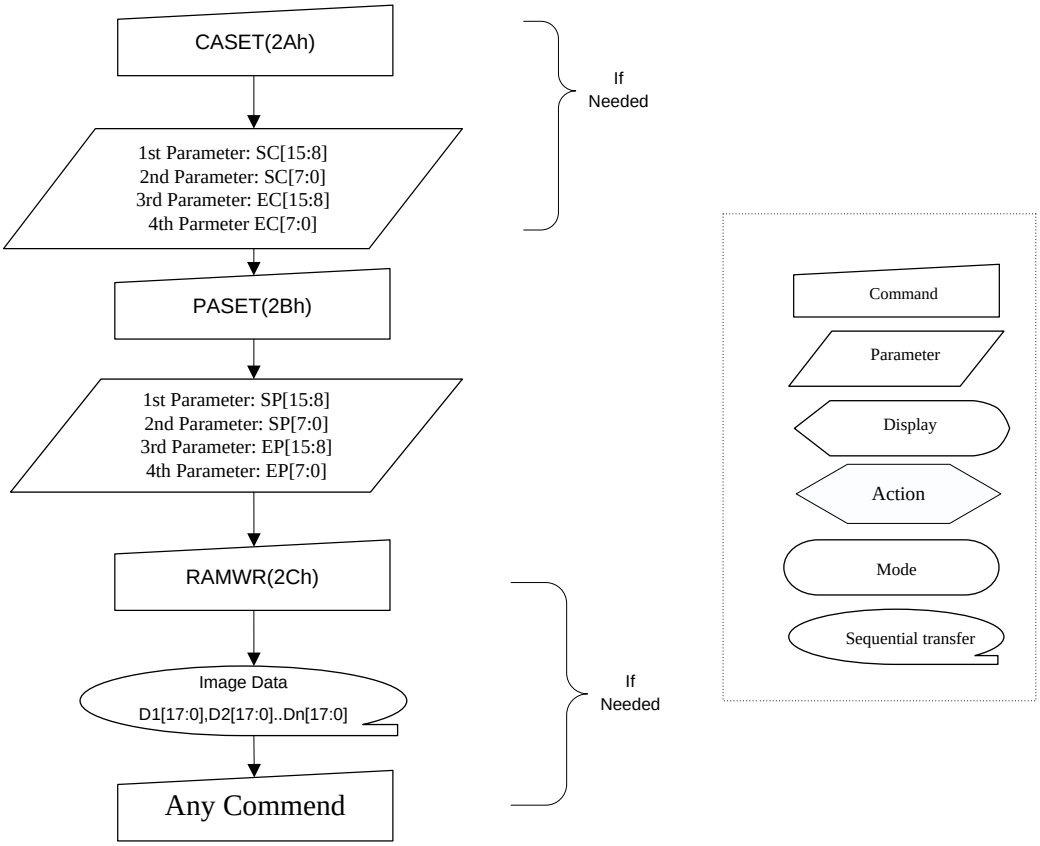
Flow Chart



5.2.12. Row Address Set (2Bh)

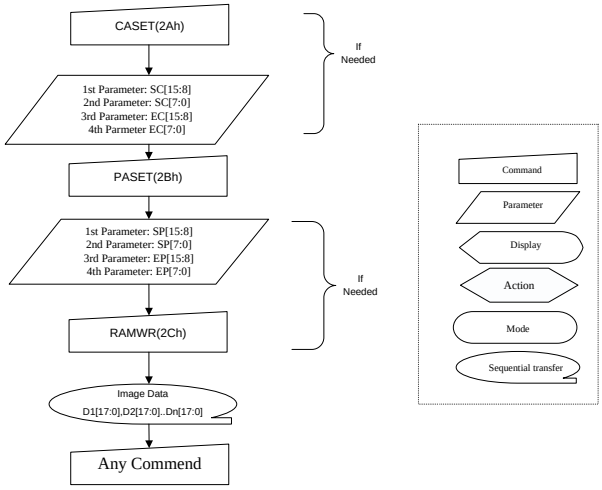
<table>
<tr><td>2Bh</td><td colspan="13">Row Address Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>2Bh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SP15</td><td>SP14</td><td>SP13</td><td>SP12</td><td>SP11</td><td>SP10</td><td>SP9</td><td>SP8</td><td rowspan="2">Note1</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SP7</td><td>SP6</td><td>SP5</td><td>SP4</td><td>SP3</td><td>SP2</td><td>SP1</td><td>SP0</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EP15</td><td>EP14</td><td>EP13</td><td>EP12</td><td>EP11</td><td>EP10</td><td>EP9</td><td>EP8</td><td rowspan="2">Note1</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EP7</td><td>EP6</td><td>EP5</td><td>EP4</td><td>EP3</td><td>EP2</td><td>EP1</td><td>EP0</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to define area of frame memory where MCU can access. This command makes no change on the
other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each value
represents one Page line in the Frame Memory.
 

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">SP [15:0] always must be equal to or less than EP [15:0]
Note 1: When SP [15:0] or EP [15:0] is greater than 00EFh (When MADCTL’s B5 = 0) or 013Fh (When MADCTL’s B5 = 1), data of out of range will be ignored.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr></table></td></tr>
</table>

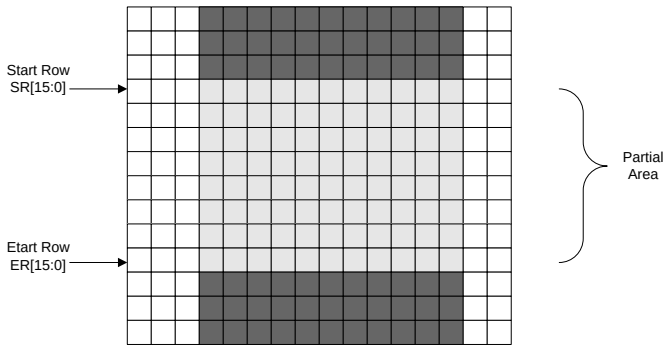
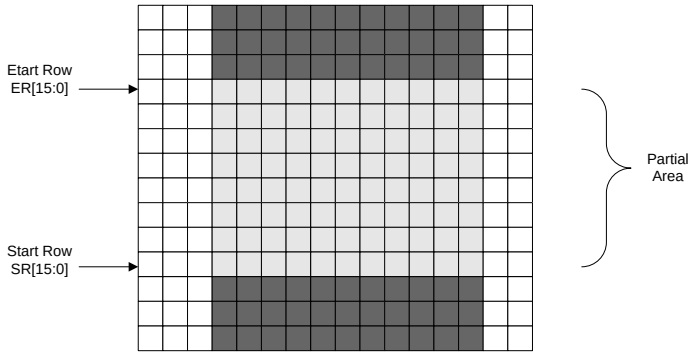
		Power On Sequence	SP [15:0]=0000h	EP [15:0]=00EFh
		SW Reset	SP [15:0]=0000h	If MADCTL's B5 = 0: EP [15:0]=0167h
				If MADCTL's B5 = 1: EP [15:0]=0167h
		HW Reset	SP [15:0]=0000h	EP [15:0]=0167h
Flow Chart				

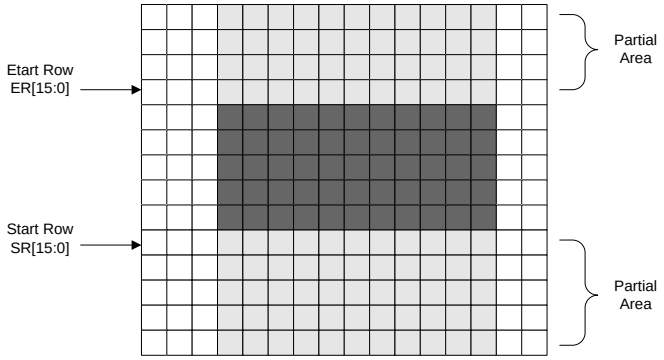
5.2.13. Memory Write (2Ch)

<table>
<tr><td>2Ch</td><td colspan="13">Memory Write</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>2Ch</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="9">D1 [17:0]</td><td>XX</td></tr>
<tr><td>:</td><td>1</td><td>1</td><td>↑</td><td colspan="9">Dx [17:0]</td><td>XX</td></tr>
<tr><td>Nth Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="9">Dn [17:0]</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver
status. When this command is accepted, the column register and the page register are reset to the Start Column/Start
Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then D [17:0] is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write. X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">In all color modes, there is no restriction on length of parameters.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>SW Reset</td><td rowspan="2">Contents of memory is not cleared</td></tr><tr><td>HW Reset</td></tr></table></td></tr>
</table>

Flow Chart	 CASET(2Ah) 1st Parameter: SC[15:8] 2nd Parameter: SC[7:0] 3rd Parameter: EC[15:8] 4th Parmeter EC[7:0] If Needed PASET(2Bh) 1st Parameter: SP[15:8] 2nd Parameter: SP[7:0] 3rd Parameter: EP[15:8] 4th Parameter: EP[7:0] If Needed RAMWR(2Ch) Image Data D1[17:0],D2[17:0]..Dn[17:0] Any Commend Command Parameter Display Action Mode Sequential transfer

5.2.14. Partial Area (30h)

30h	Partial Area												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
1st Parameter	1	1	↑	XX	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00
2nd Parameter	1	1	↑	XX	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
3rd Parameter	1	1	↑	XX	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	01
4th Parameter	1	1	↑	XX	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	67
Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row>Start Row when MADCTL B4=0:-  If End Row>Start Row when MADCTL B4=1:-  If End Row<Start Row when MADCTL B4=0:-												



If End Row = Start Row then the Partial Area will be one row deep.

X = Don't care.

Restriction	SR [15…0] and ER [15…0] cannot be 0000h nor exceed 0167h.

Register Availability

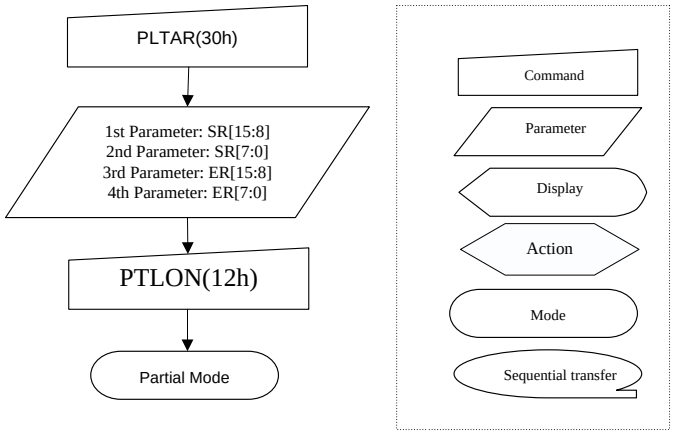
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

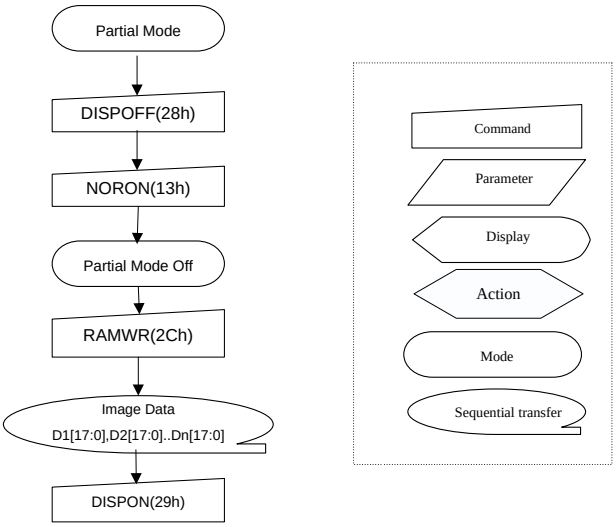
Status	Default Value	
	SR [15:0]	ER [15:0]
Power On Sequence	16'h0000h	16'h0167h
SW Reset	16'h0000h	16'h0167 h
HW Reset	16'h0000h	16'h0167 h

Flow Chart

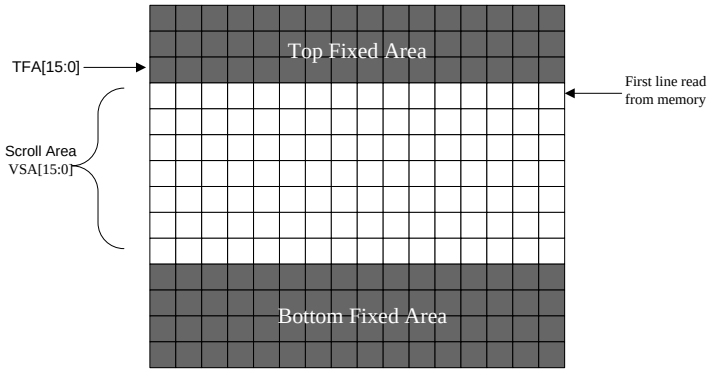
1. To Enter Partial Mode

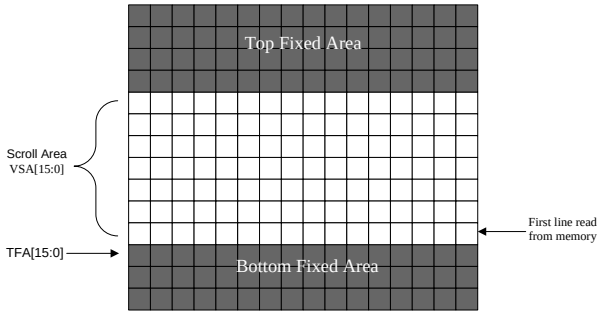


2. To Leave Partial Mode



5.2.15. Vertical Scrolling Definition (33h)

33h	Vertical Scrolling Definition												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
1st Parameter	1	1	↑	XX	TFA [15:8]								00
2nd Parameter	1	1	↑	XX	TFA [7:0]								00
3rd Parameter	1	1	↑	XX	VSA [15:8]								01
4th Parameter	1	1	↑	XX	VSA [7:0]								67
Description	This command defines the Vertical Scrolling Area of the display. When MADCTL B4=0 The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display). The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.  When MADCTL B4=1 The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.												



X = Don’t care.

Restriction

Register Availability

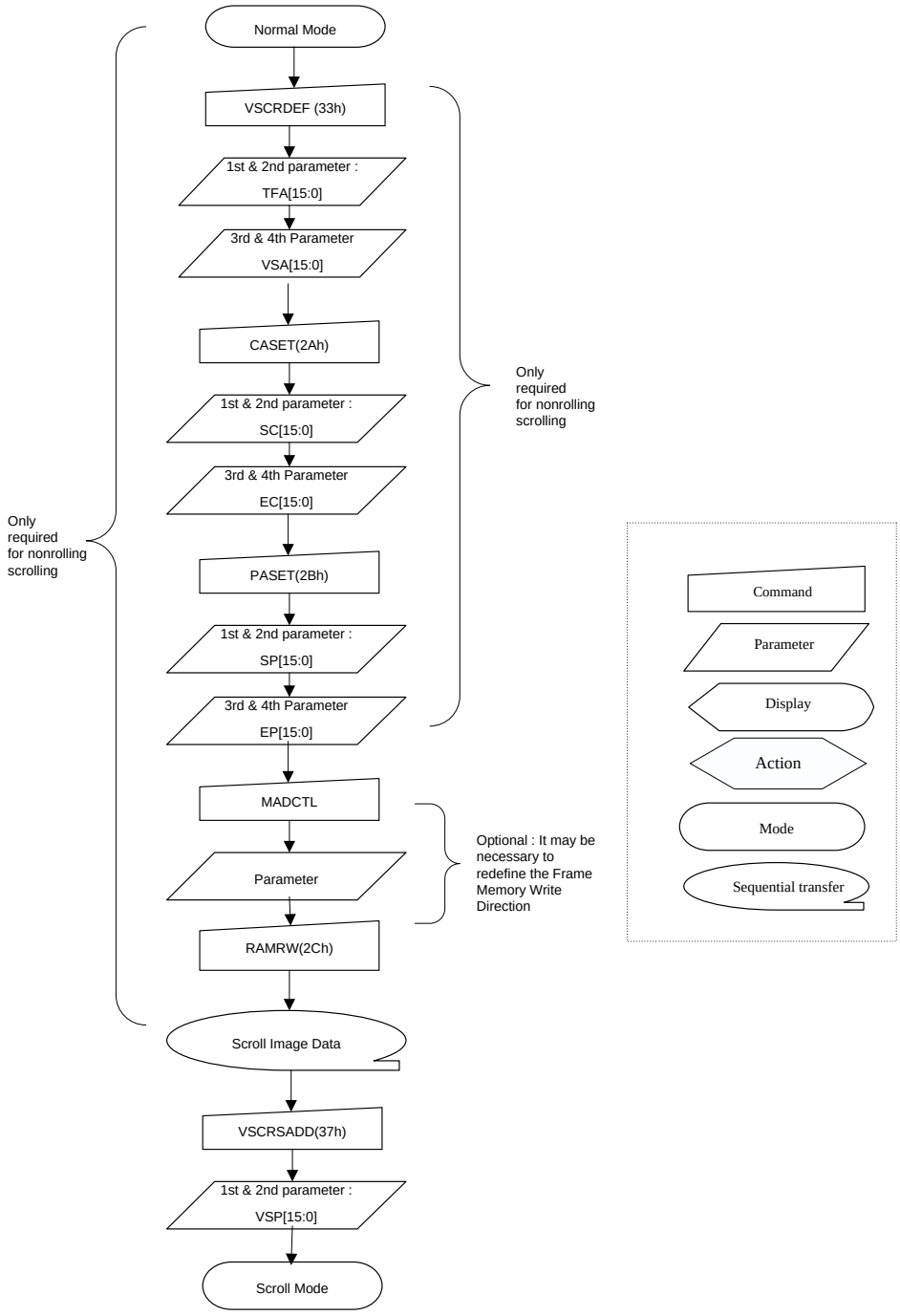
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	TFA [15:0]	VSA [15:0]
Power On Sequence	16’h0000h	16’h0167h
SW Reset	16’h0000h	16’h0167h
HW Reset	16’h0000h	16’h0167h

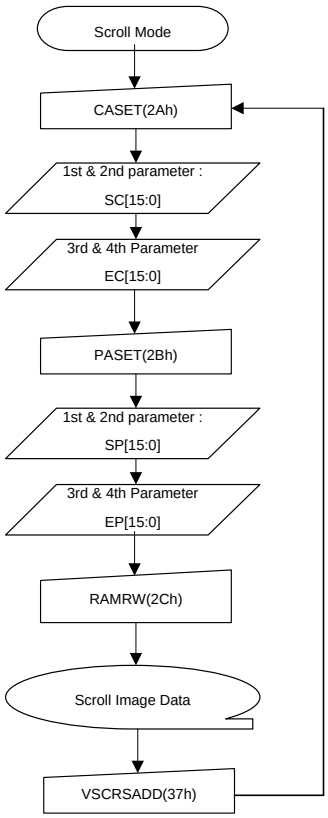
Flow Chart

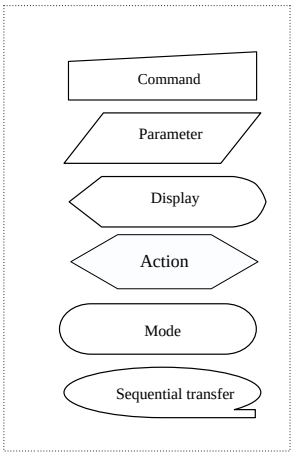
1. To enter Vertical Scroll Mode :



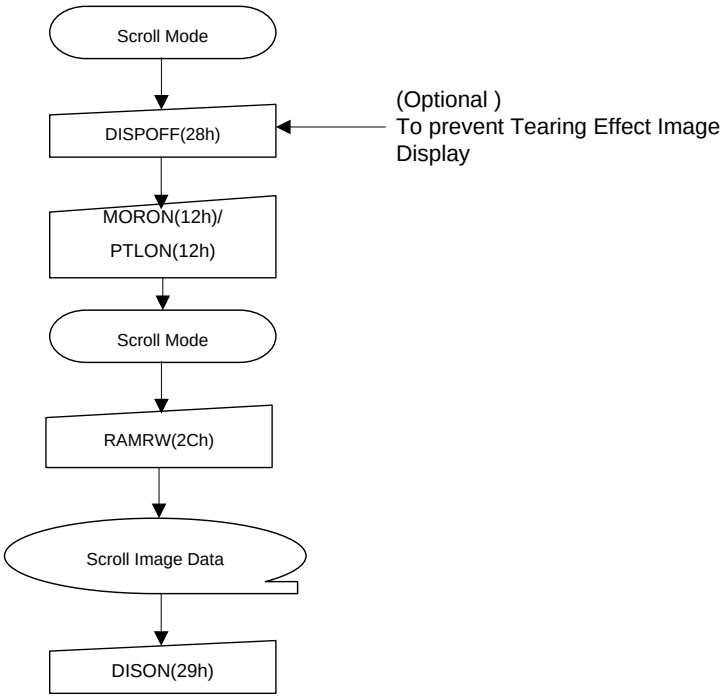
Note : The Frame Memory Window size ,must be defined correctly otherwise undesirable image will be displayed.

2.Continuous Scroll :



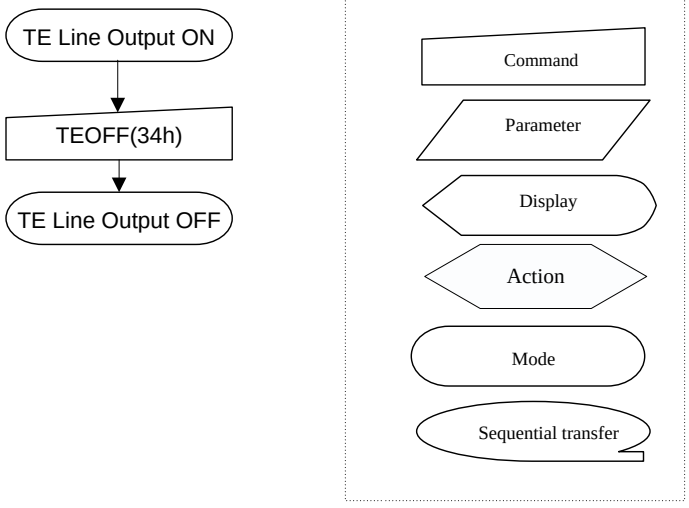


3.To Leave Vertical Scroll Mode:



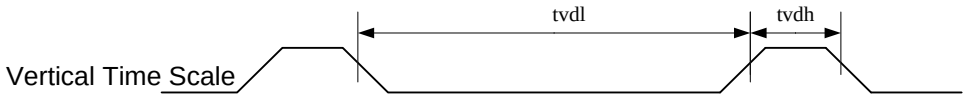
Note: Scroll Mode can be left by both the Normal Display Mode ON (13h) and Partial Mode ON (12h) commands.

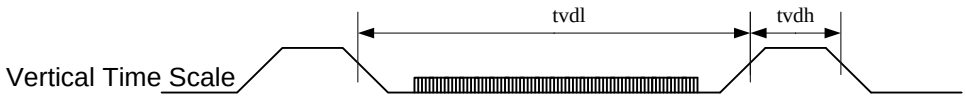
5.2.16. Tearing Effect Line OFF (34h)

<table>
<tr><td>34h</td><td colspan="13">Tearing Effect Line OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>34h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already OFF.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

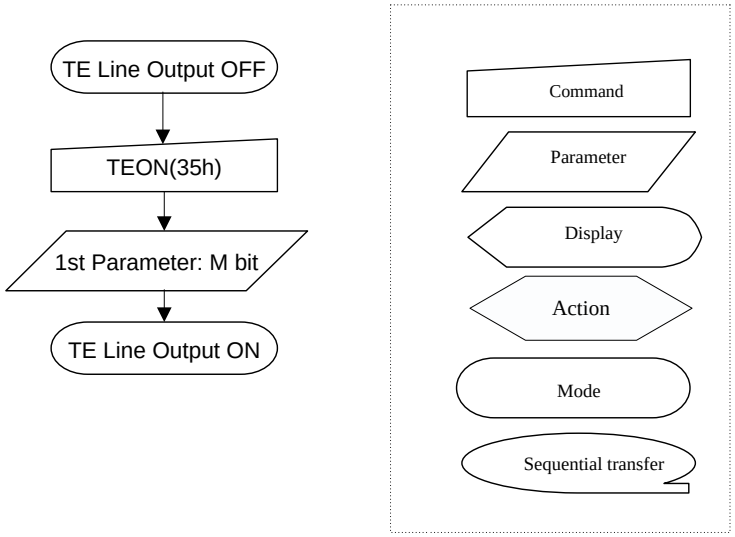
5.2.17. Tearing Effect Line ON (35h)

<table>
<tr><td>35h</td><td colspan="13">Tearing Effect Line ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>35h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>M</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by
changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When M=0:
The Tearing Effect Output line consists of V-Blanking information only:
 

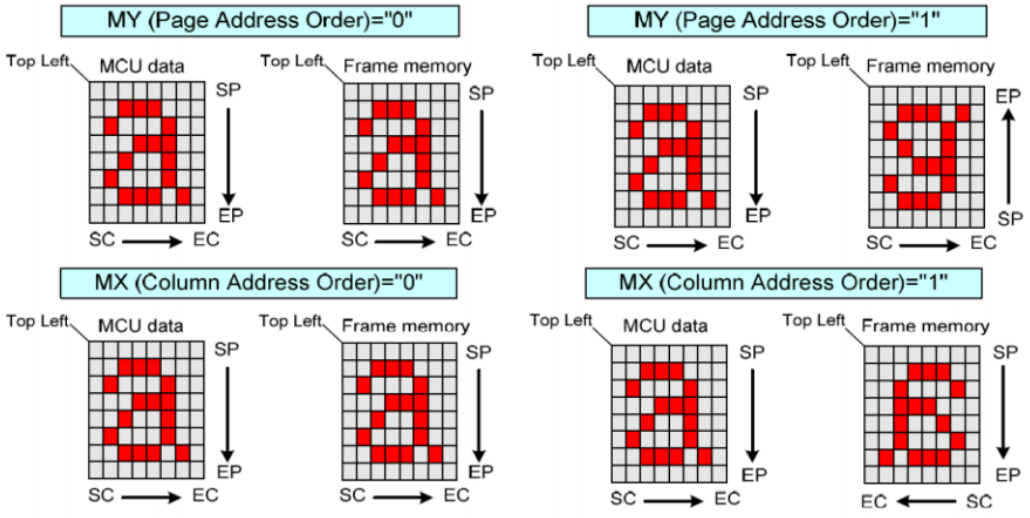
When M=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:
 

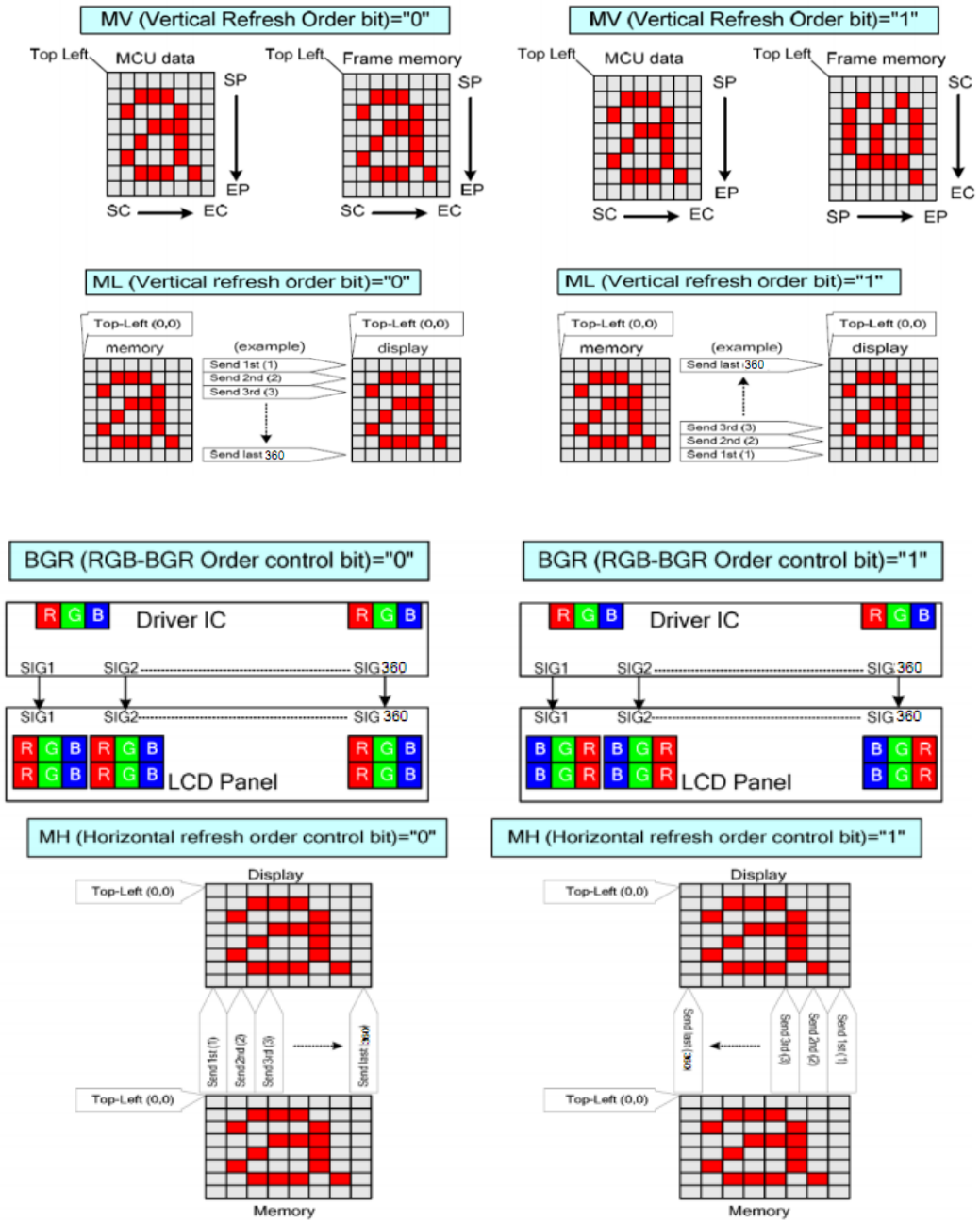
Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already ON</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table></td></tr>
</table>

Flow Chart	

TE Line Output OFF
TEON(35h)
1st Parameter: M bit
TE Line Output ON
Command
Parameter
Display
Action
Mode
Sequential transfer

5.2.18. Memory Access Control(36h)

<table>
<tr><td>36h</td><td colspan="13">Tearing Effect Line ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>36h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>MY</td><td>MX</td><td>MV</td><td>ML</td><td>BGR</td><td>MH</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.
<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>MY</td><td>Row Address Order</td><td rowspan="3">These 3 bits control MCU to memory write/read direction.</td></tr>
<tr><td>MX</td><td>Column Address Order</td></tr>
<tr><td>MV</td><td>Row / Column Exchange</td></tr>
<tr><td>ML</td><td>Vertical Refresh Order</td><td>LCD vertical refresh direction control.</td></tr>
<tr><td>BGR</td><td>RGB-BGR Order</td><td>Color selector switch control
(0=RGB color filter panel, 1=BGR color filter panel)</td></tr>
<tr><td>MH</td><td>Horizontal Refresh ORDER</td><td>LCD horizontal refreshing direction control.</td></tr>
</table>
Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.

</td></tr>
</table>



Note: Top-Left (0,0) means a physical memory location.

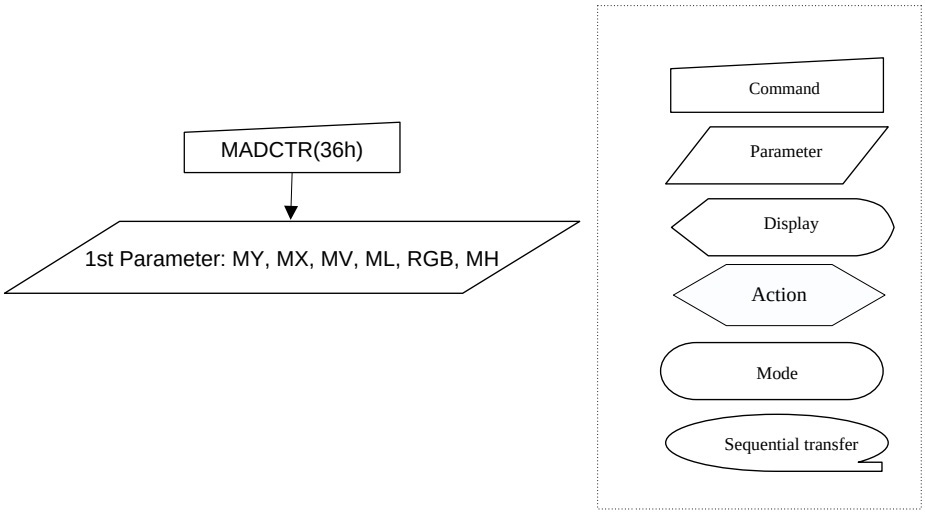
Restriction	This command has no effect when Tearing Effect output is already ON

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value

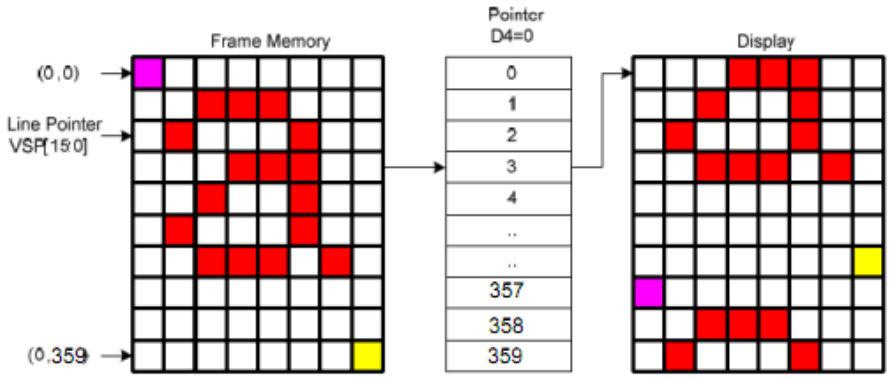
	Power On Sequence: 8'h00h SW Reset: No change HW Reset: 8'h00h
Flow Chart	

5.2.19. Vertical Scrolling Start Address (37h)

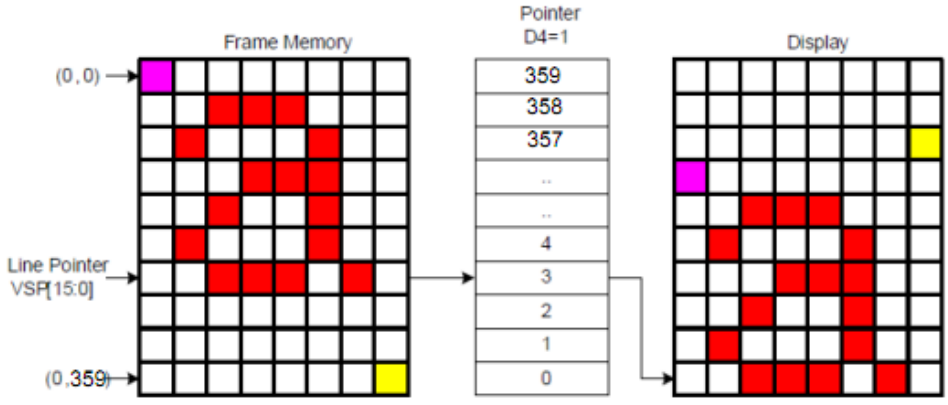
37h	VSCRSADD (Vertical Scrolling Start Address)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
1st Parameter	1	1	↑	XX	VSP [15:8]								00
2nd Parameter	1	1	↑	XX	VSP [7:0]								00

Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area
and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-
When MADCTL B4=0
Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 360 and VSP='3'.



When MADCTL B4=1
Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 360 and VSP='3'.

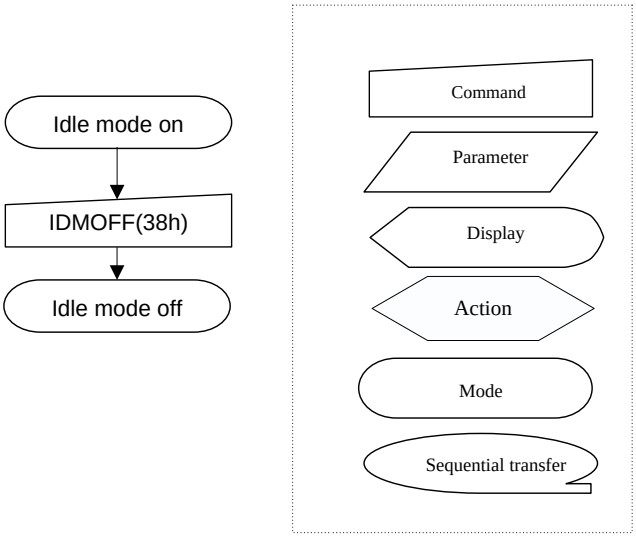


Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line

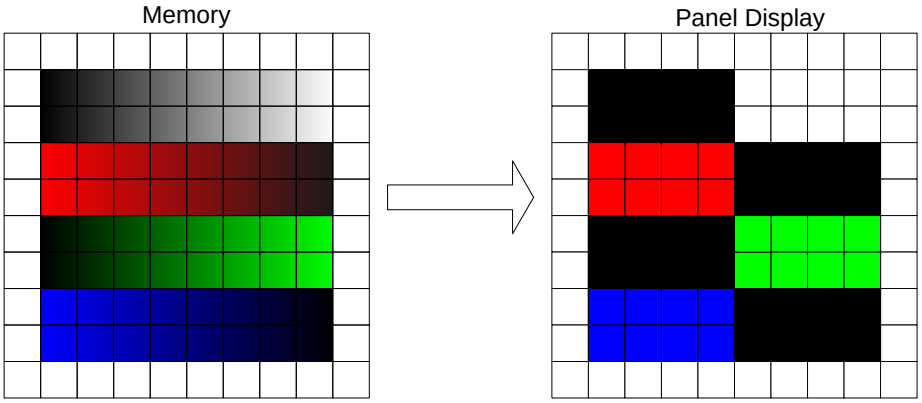
	Pointer. *(2) This command is ignored when the GC9B71 enters Partial mode.* X = Don’t care
Restriction	This command has no effect when Tearing Effect output is already ON

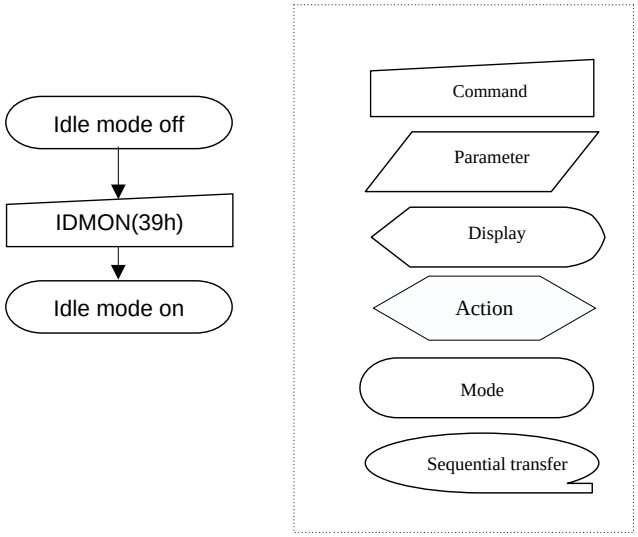
<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VSP [15:0]</th></tr>
<tr><td>Power On Sequence</td><td>16’h0000h</td></tr>
<tr><td>SW Reset</td><td>16’h0000h</td></tr>
<tr><td>HW Reset</td><td>16’h0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

5.2.20. Idle Mode OFF (38h)

<table>
<tr><td>38h</td><td colspan="13">Idle Mode OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>38h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from Idle mode on.
In the idle off mode, LCD can display maximum 262,144 colors.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle mode OFF</td></tr><tr><td>SW Reset</td><td>Idle mode OFF</td></tr><tr><td>HW Reset</td><td>Idle mode OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

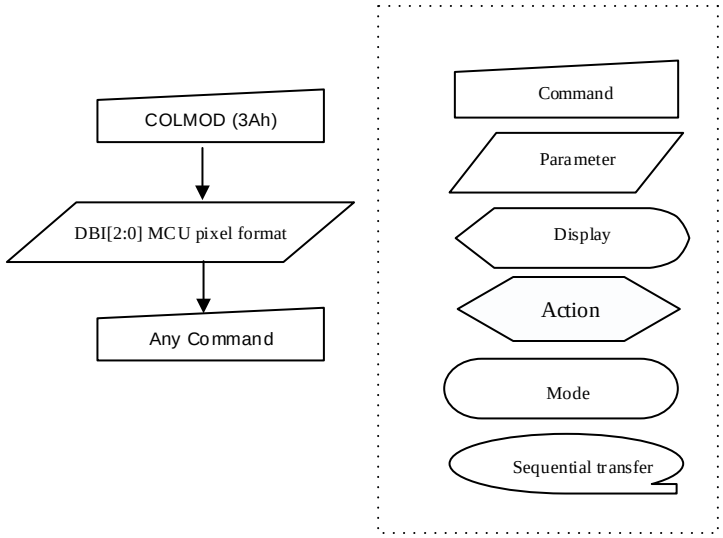
5.2.21. Idle Mode ON (39h)

<table>
<tr><td>39h</td><td colspan="13">Idle Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>39h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enter into Idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.
 
<table><tr><td></td><td colspan="3">Memory Contents vs. Display Color</td></tr><tr><td></td><td>R5 R4 R3 R2 R1 R0</td><td>G5 G4 G3 G2 G1 G0</td><td>B5 B4 B3 B2 B1 B0</td></tr><tr><td>Black</td><td>0XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr><tr><td>Blue</td><td>0XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr><tr><td>Red</td><td>1XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr><tr><td>Magenta</td><td>1XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr><tr><td>Green</td><td>0XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr><tr><td>Cyan</td><td>0XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr><tr><td>Yellow</td><td>1XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr><tr><td>White</td><td>1XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr></table>X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

<table>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Idle mode OFF</td></tr>
<tr><td>SW Reset</td><td>Idle mode OFF</td></tr>
<tr><td>HW Reset</td><td>Idle mode OFF</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

5.2.22. COLMOD: Pixel Format Set (3Ah)

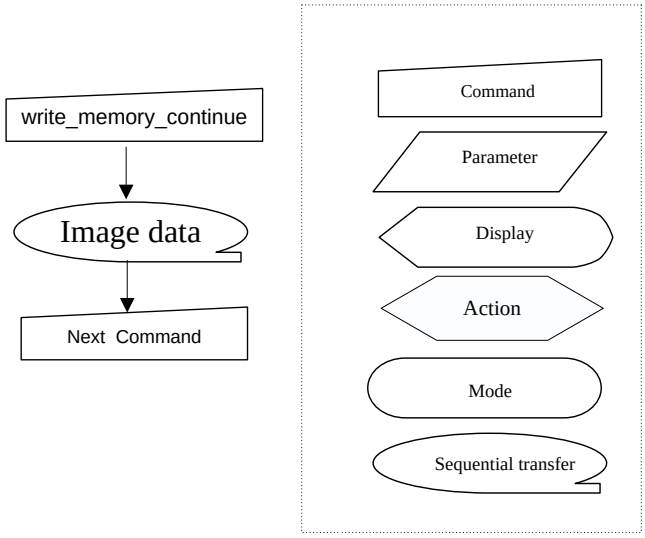
<table>
<tr><td>3Ah</td><td colspan="13">Pixel Format Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3Ah</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td colspan="3">DBI [2:0]</td><td>66</td></tr>
<tr><td>Description</td><td colspan="13">This command sets the pixel format for the RGB image data used by the interface. DBI [2:0] is the pixel format of MCU interface. The pixel format is shown in the table below.
<table>
<tr><th colspan="3">DBI [2:0]</th><th>MCU Interface Format</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Gray256（QSPI only）</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>3bits/ pixel（QSPI only）</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>8bits/ pixel（QSPI only）</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>12 bits / pixel</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>24bits/pixel
（QSPI &dither on）</td></tr>
</table>
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>DPI [2:0]</th><th>DBI [2:0]</th></tr>
<tr><td>Power On Sequence</td><td>3’b110</td><td>3’b110</td></tr>
<tr><td>SW Reset</td><td>No Change</td><td>No Change</td></tr>
<tr><td>HW Reset</td><td>3’b110</td><td>3’b110</td></tr>
</table>
</td></tr>
</table>

Flow Chart	 COLMOD (3Ah) DBI[2:0] MCU pixel format Any Command Command Parameter Display Action Mode Sequential transfer

5.2.23. Write Memory Contiue (3Ch)

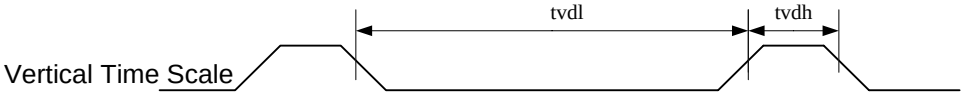
3Ch	write_memory_continue												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	D1[17..8]	0	0	1	1	1	1	0	0	3Ch
1st Parameter	1	1	↑	Dx[17..8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	0003FF
Xth Parameter	1	1	↑	D1[17..8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	0003FF
Nth Parameter	1	1	↑	Dn[17..8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	0003FF
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. **If set_address_mode B5 = 0:** Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC –SC + 1) * (EP – SP + 1) the extra pixels are ignored. **If set_address_mode B5 = 1:** Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP –SP + 1) the extra pixels are ignored. Sending any other command can stop frame Write. Frame Memory Access and Interface setting (B3h), WEMODE=0 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored. Frame Memory Access and Interface setting (B3h), WEMODE=1 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.												

Restriction	A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.

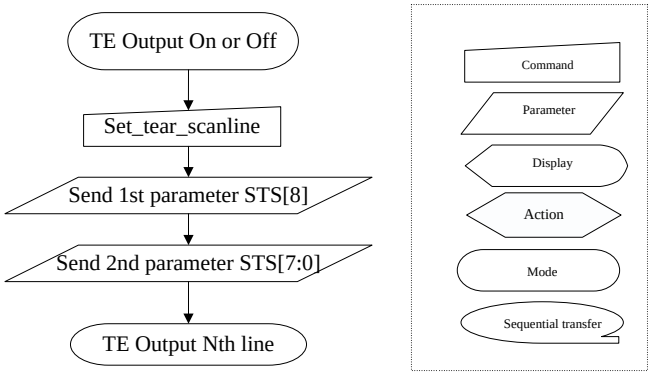
<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Random value</td></tr>
<tr><td>SW Reset</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>No change</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>


</td></tr>
</table>

5.2.24. Set_Tear_Scanline (44h)

<table>
<tr><td>44h</td><td colspan="13">Set_Tear_Scanline</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>44h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>STS [8]</td><td>00</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>STS [7]</td><td>STS [6]</td><td>STS [5]</td><td>STS [4]</td><td>STS [3]</td><td>STS [2]</td><td>STS [1]</td><td>STS [0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line equal the value of STS[8:0]
 

Note:that set_tear_scanline with STS is equivalent to set_tear_on with 8+GateN(N=1、2、3...260)
eg:when the STS[8:0]=8,the TE will output at the position of Gate1.
when the STS[8:0]=9,the TE will output at the position of Gate2.
when the STS[8:0]=10,the TE will output at the position of Gate3.
…….
The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>STS [8:0]=0000h</td></tr><tr><td>SW Reset</td><td>STS [8:0]=0000h</td></tr><tr><td>HW Reset</td><td>STS [8:0]=0000h</td></tr></table></td></tr>
</table>

Flow Chart	 TE Output On or Off Set_tear_scanline Send 1st parameter STS[8] Send 2nd parameter STS[7:0] TE Output Nth line Command Parameter Display Action Mode Sequential transfer

5.2.25. Get_Scanline (45h)

45h	Get_Scanline												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
1st Parameter	1	↑	1	XX	0	0	0	0	0	0	0	GTS [8]	00
2nd Parameter	1	↑	1	XX	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	00
Description	This command returns the setting value of STS[8:0] . When in Sleep Mode, the value returned by get_scanline is undefined.												
Restriction	None												

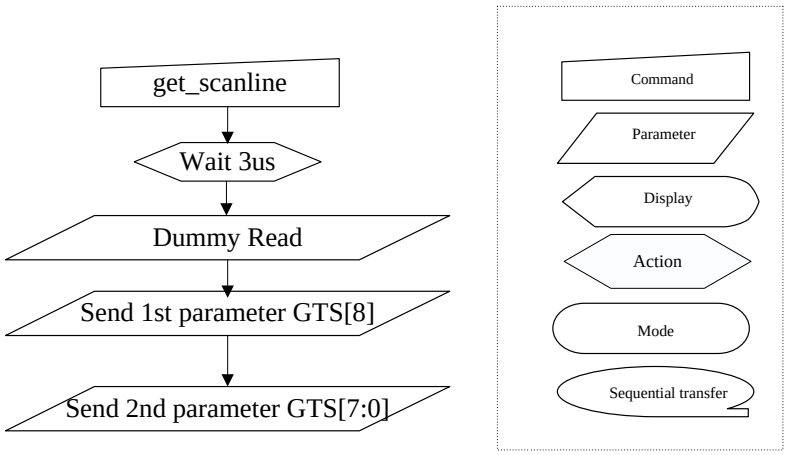
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	GTS [9:0]=0000h
SW Reset	GTS [9:0]=0000h
HW Reset	GTS [9:0]=0000h

Flow Chart



5.2.26. Write Display Brightness (51h)

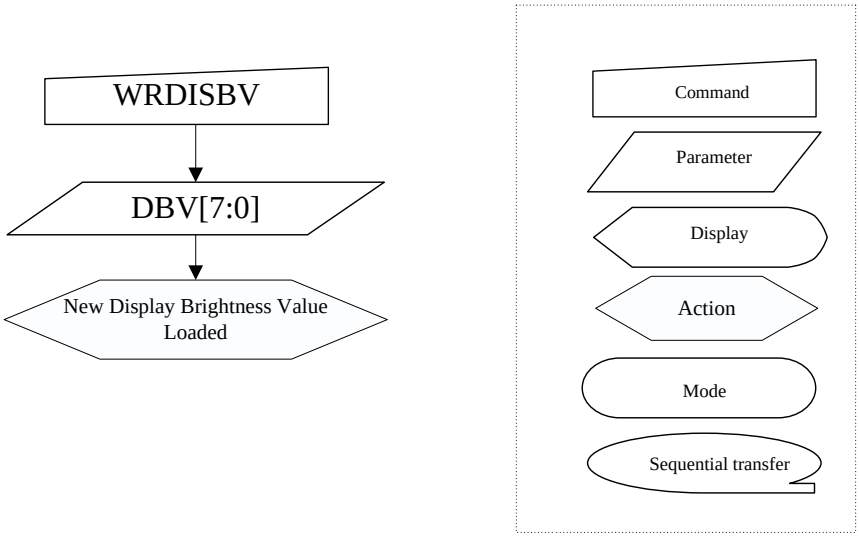
51h	Write Display Brightness												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	0	0	1	51h
1st Parameter	1	1	↑	XX	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[6]	DBV[5]	DBV[4]	00
Description	This command is used to adjust the brightness value of the display. It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.												
Restriction	None												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

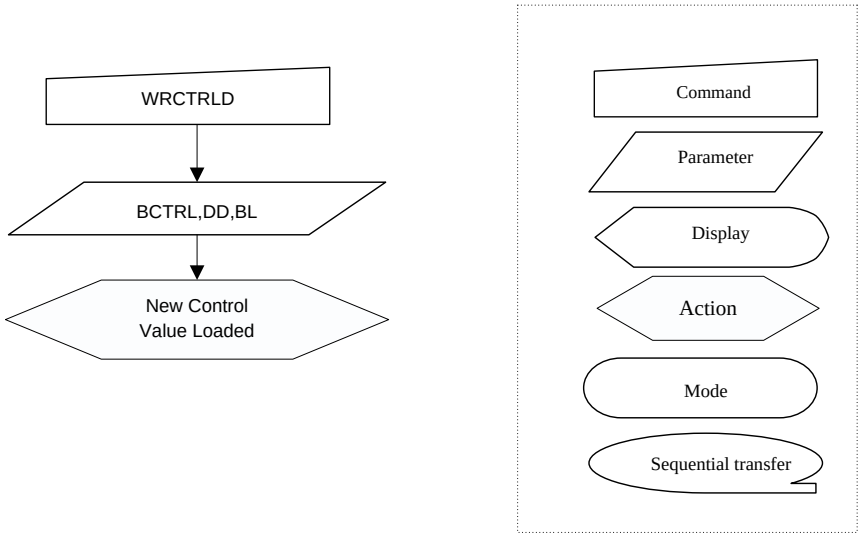
Status	Default Value
Power On Sequence	DBV [7:0]= 8'h00
SW Reset	DBV [7:0]= 8'h00
HW Reset	DBV [7:0]= 8'h00

Flow Chart	

WRDISBV
DBV[7:0]
New Display Brightness Value Loaded
Command
Parameter
Display
Action
Mode
Sequential transfer

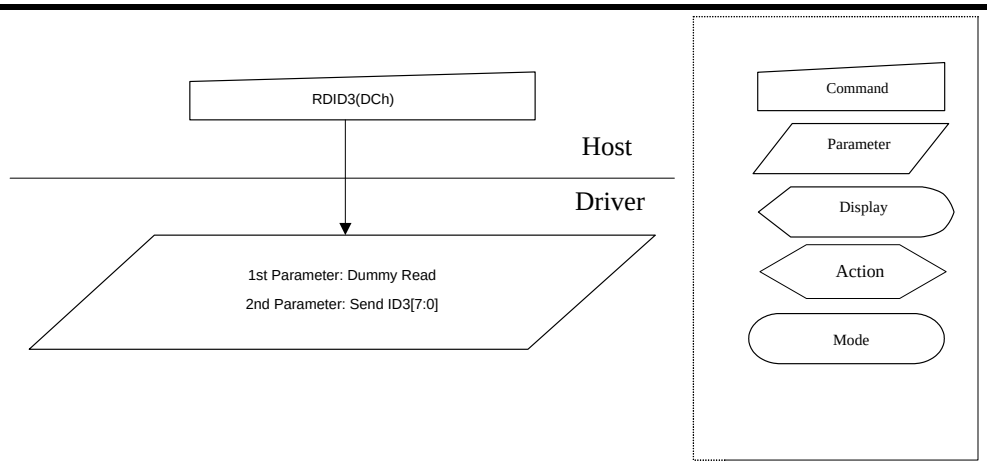
5.2.27. Write CTRL Display (53h)

<table>
<tr><td>53h</td><td colspan="13">Write CTRL Display</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>53h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>BCTRL</td><td>0</td><td>DD</td><td>BL</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to return brightness setting.
BCTRL: Brightness Control Block On/Off,
‘0’ = Off (Brightness registers are 00h)
‘1’ = On (Brightness registers are active, according to the DBV[7..0] parameters.)
DD: Display Dimming
‘0’ = Display Dimming is off
‘1’ = Display Dimming is on
BL: Backlight On/Off
‘0’ = Off (Completely turn off backlight circuit. Control lines must be low.)
‘1’ = On</td></tr>
<tr><td>Restriction</td><td colspan="13">The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter
(= more than 2 RDX cycle) on DBI.
Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>BCTRL</th><th>DD</th><th>BL</th></tr><tr><td>Power On Sequence</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr><tr><td>SW Reset</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr><tr><td>HW Reset</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr></table></td></tr>
</table>

Flow Chart	 WRCTRLD BCTRL,DD,BL New Control Value Loaded Command Parameter Display Action Mode Sequential transfer

5.2.28. Read ID1 (DAh)

<table>
<tr><td>DCh</td><td colspan="13">Read ID2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>DAh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="9">ID3 [7:0]</td><td>Program value</td></tr>
<tr><td>Description</td><td colspan="13">This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User’s agreement) and changes each time a revision is made to the display, material or construction specifications.
The 1st parameter is dummy data.
The 2nd parameter is LCD module/driver version ID
The ID3 can be programmed by MTP function.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value (After MTP program)</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>SW Reset</td><td>8’h00</td></tr><tr><td>HW Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

Flow Chart	 RDID3(DCh) Host Driver 1st Parameter: Dummy Read 2nd Parameter: Send ID3[7:0] Command Parameter Display Action Mode

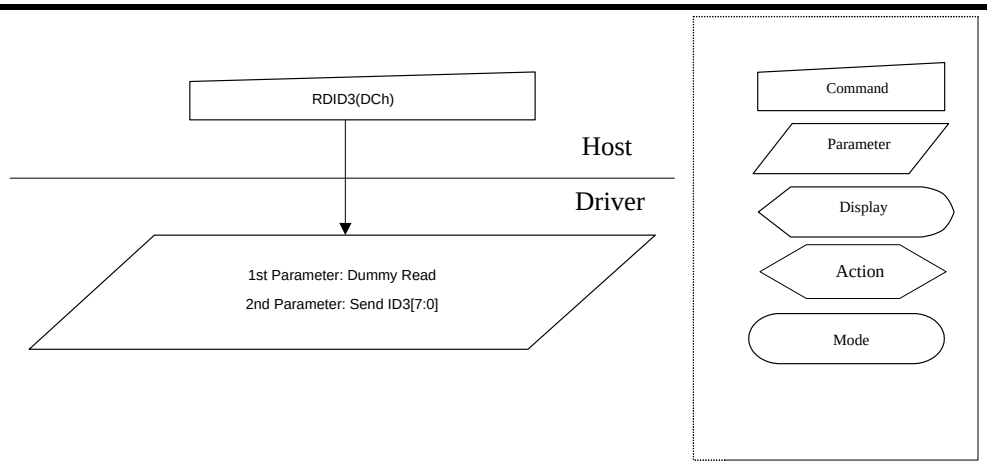
5.2.29. Read ID2 (DBh)

DCh	Read ID2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID3 [7:0]								Program value
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID The ID3 can be programmed by MTP function. X = Don't care												
Restriction	None												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

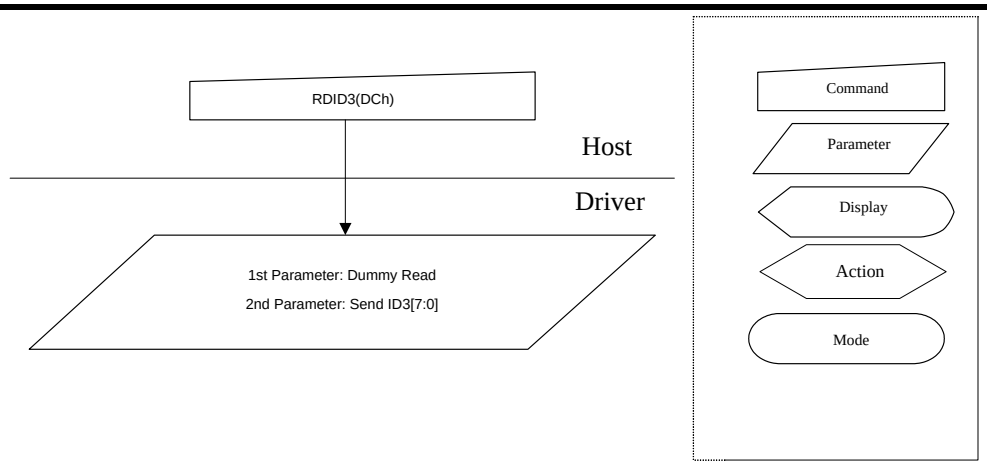
Default

Status	Default Value (After MTP program)
Power On Sequence	8'h9B
SW Reset	8'h9B
HW Reset	8'h9B

Flow Chart	 RDID3(DCh) Host Driver 1st Parameter: Dummy Read 2nd Parameter: Send ID3[7:0] Command Parameter Display Action Mode

5.2.30. Read ID3 (DCh)

<table>
<tr><td>DCh</td><td colspan="13">Read ID2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>DCh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID3 [7:0]</td><td>Program value</td></tr>
<tr><td>Description</td><td colspan="13">This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User’s agreement) and changes each time a revision is made to the display, material or construction specifications.
The 1st parameter is dummy data.
The 2nd parameter is LCD module/driver version ID
The ID3 can be programmed by MTP function.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value (After MTP program)</th></tr><tr><td>Power On Sequence</td><td>8’h71</td></tr><tr><td>SW Reset</td><td>8’h71</td></tr><tr><td>HW Reset</td><td>8’h71</td></tr></table></td></tr>
</table>

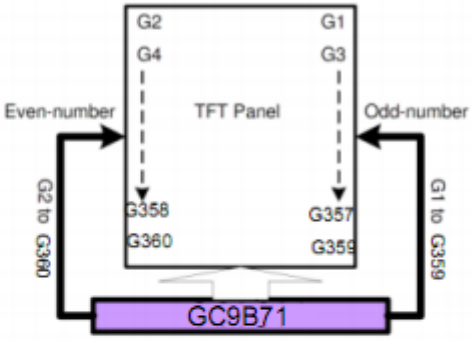
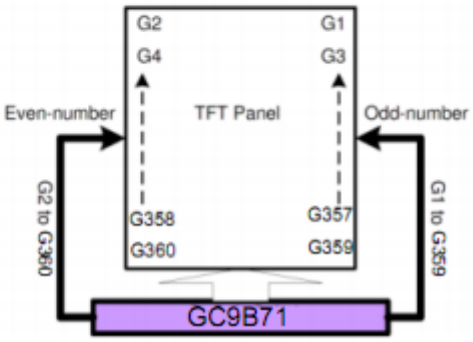
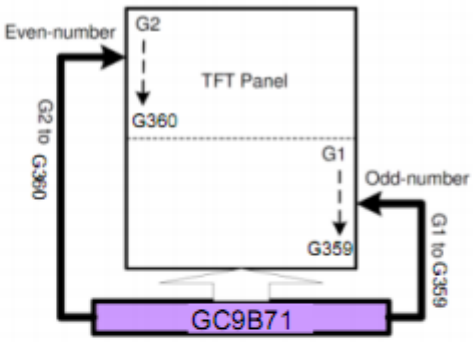
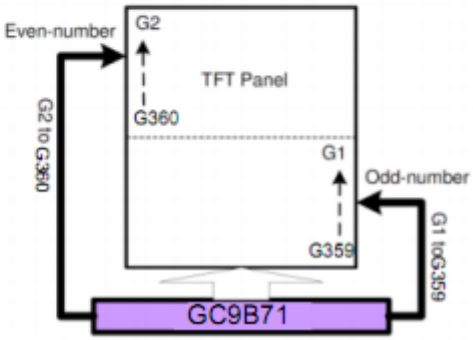
Flow Chart	 RDID3(DCh) Host Driver 1st Parameter: Dummy Read 2nd Parameter: Send ID3[7:0] Command Parameter Display Action Mode

5.3. Description of Level 2 Command

5.3.1. Display Function Control (B6h)

<table>
<tr><td>B6h</td><td colspan="13">Display Function Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>B6h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>GS</td><td>SS</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">
note:the first parameter must write,but it is not valid.
SS: Select the shift direction of outputs from the source driver.
<table>
<tr><th>SS</th><th>Source Output Scan Direction</th></tr>
<tr><td>0</td><td>S1 → S540</td></tr>
<tr><td>1</td><td>S540 → S1</td></tr>
</table>
In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, and B dots to the source driver pins.
To assign R, G, B dots to the source driver pins from S1 to S360, set SS = 0.
To assign R, G, B dots to the source driver pins from S360 to S1, set SS = 1.

GS: Sets the direction of scan by the gate driver in the range determined by SCN [4:0] and NL [4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.
<table>
<tr><th>GS</th><th>Gate Output Scan Direction</th></tr>
<tr><td>0</td><td>G1→G360</td></tr>
<tr><td>1</td><td>G360→G1</td></tr>
</table>
</td></tr>
</table>

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1→G2→G3→G4→ ....→G357→G358→G359→G360
0	1		G360 →G359→G358→G357→..... .... →G4→G3→G2→G1
1	0		G1→G3→.....→G357→G359→ G2→G4→.....→G358→G360
1	1		G360→G358→.....→G4→G2→ G359→G357→.....→G3→G1

NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected
by the number of lines set by NL [5:0]. The number of lines must be the same or more than the number of lines necessary
for the size of the liquid crystal panel.

NL [5:0]	LCD Drive Line	NL [5:0]	LCD Drive Line

		0	0	0	0	0	0	Setting prohibited		0	1	0	1	0	1	176 lines
		0	0	0	0	0	1	16 lines		0	1	0	1	1	0	184 lines
		0	0	0	0	1	0	24 lines		0	1	0	1	1	1	192 lines
		0	0	0	0	1	1	32 lines		0	1	1	0	0	0	200 lines
		0	0	0	1	0	0	40 lines		0	1	1	0	0	1	208 lines
		0	0	0	1	0	1	48 lines		.....						
		0	0	0	1	1	0	56 lines		1	1	0	0	1	1	344 lines
		0	0	0	1	1	1	64 lines		1	1	0	1	0	0	352 lines
		0	0	1	0	0	0	72 lines		1	1	0	1	0	1	360 lines
		0	0	1	0	0	1	80 lines		Others						Setting prohibited
		0	0	1	0	1	0	88 lines								
		0	0	1	0	1	1	96 lines								
		0	0	1	1	0	0	104 lines								
		0	0	1	1	0	1	112 lines								
		0	0	1	1	1	0	120 lines								
		0	0	1	1	1	1	128 lines								
		0	1	0	0	0	0	136 lines								
		0	1	0	0	0	1	144 lines								
		0	1	0	0	1	0	152 lines								
		0	1	0	0	1	1	160 lines								

Restriction	EXTC should be high to enable this command

Register Availability

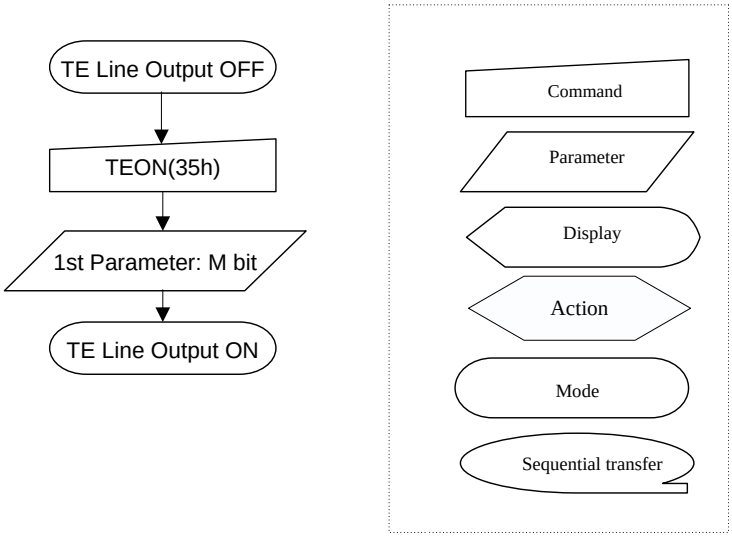
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	-	GS	SS	/
Power On Sequence	-	1'b0	1'b0	/
HW Reset	-	1'b0	1'b0	/

5.4. Tearing Effect Control (B4h)

<table>
<tr><td>B4h</td><td colspan="13">Tearing Effect Width Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>B4h</td></tr>
<tr><td>Parameter1</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">te_width[7:0]</td><td>00</td></tr>
<tr><td>Parameter2</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>te_pol</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">te_pol is used to adjust the Tearing Effect output signal pulse polarity.
<table><tr><th>te_pol</th><th>Tearing Effect polarity</th></tr><tr><td>0</td><td>Positive pulse</td></tr><tr><td>1</td><td>negative pulse</td></tr></table>te_width[6:0] is used to adjust the Tearing Effect output signal pulse width with display lines in unit
<table><tr><th>te_width[7:0]</th><th>Tearing Effect width(display line time)</th></tr><tr><td>0</td><td>1line time</td></tr><tr><td>1</td><td>2line time</td></tr><tr><td>…</td><td>…</td></tr><tr><td>N</td><td>N+1 line time</td></tr><tr><td>…</td><td>…</td></tr><tr><td>7f</td><td>128 line time</td></tr></table>Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already ON</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>0x00</td></tr><tr><td>SW Reset</td><td>0x00</td></tr><tr><td>HW Reset</td><td>0x00</td></tr></table></td></tr>
</table>

Flow Chart	

TE Line Output OFF
TEON(35h)
1st Parameter: M bit
TE Line Output ON
Command
Parameter
Display
Action
Mode
Sequential transfer

5.5. Description of Level 3 Command

5.5.1. Inversion (ECh)

<table>
<tr><td>ECh</td><td colspan="13">Iversion</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>ECh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td colspan="3">DINV[2:0]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0x70</td></tr>
<tr><td>Description</td><td colspan="13">DINV[2:0] : Set display inversion mode
<table><tr><th>DINV[2:0]</th><th>Inversion</th></tr><tr><td>0</td><td>1+2H1V</td></tr><tr><td>1</td><td>Column</td></tr><tr><td>2</td><td>2H1V</td></tr><tr><td>3</td><td>reserved</td></tr><tr><td>4</td><td>reserved</td></tr><tr><td>7</td><td>2 column inversion</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

Default	<table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><th>DINV[2:0]</th></tr><tr><td>Power On Sequence</td><td>4'h1</td></tr><tr><td>SW Reset</td><td>4'h1</td></tr><tr><td>HW Reset</td><td>4'h1</td></tr></table>

5.5.2.SPI 2DATA control(B1h)

B1h	SPI 2DATA control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h
1st Parameter	1	1	↑	XX	X	X	X	DTR_EN	2data_en	2data_mdt[2:0]			00
Description	**DTR_EN:** Dithering enable. **2DATA_EN:** Set 2_data_line mode in 3-wire/4-wire SPI. **2DATA_MDT[2:0]** Set pixel data format in 2_data_line mode. <table><tr><th>2DATA_MDT[2:0]</th><th>Data Format</th></tr><tr><td>000</td><td>65K color 1pixle/transition</td></tr><tr><td>001</td><td>262K color 1pixle/transition</td></tr><tr><td>010</td><td>262K color 2/3pixle/transition</td></tr></table>												
Restriction	Inter command should be set high to enable this command												
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>												
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>2DATA_EN</th><th>2DATA_MDT[2:0]</th></tr><tr><td>Power On Sequence</td><td>1'b0</td><td>3'b000</td></tr><tr><td>SW Reset</td><td>1'b0</td><td>3'b000</td></tr><tr><td>HW Reset</td><td>1'b0</td><td>3'b000</td></tr></table>												

5.5.3.Power Control 1 (C1h)

<table>
<tr><td>C1h</td><td colspan="12">Power Control 1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>C1h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>vcire</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="12">vcire: Select the external reference voltage VDDB or internal reference voltage VDDBR.
<table><tr><td>vcire =0</td><td>Internal reference voltage 2.5V (default)</td></tr><tr><td>vcire =1</td><td>External reference voltage VDDB</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="12">Inter_command should be set high to enable this command</td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td rowspan="2">Status</td><td>Default Value</td></tr><tr><td>vcire</td></tr><tr><td>Power On Sequence</td><td>1’b0</td></tr><tr><td>SW Reset</td><td>1’b0</td></tr><tr><td>HW Reset</td><td>1’b0</td></tr></table></td></tr>
</table>

5.5.4.Power Control 2 (C3h)

<table>
<tr><td>C3h</td><td colspan="12">Power Control 2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>C3h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="7">vreg1_vbp_d[6:0]</td><td>3C</td></tr>
<tr><td>Description</td><td colspan="12">Set the voltage level value to output the VREG1A and VREG1B OUT level, which is a reference level for the grayscale voltage level.(Table is valid when vrh=0x28)
VREG1A=(vrh+vbp_d)*0.02+4
VREG1B=vbp_d*0.02+0.3
<table>
<tr><th>vreg1_vbp_d[6:0]</th><th>VREG1A/V</th><th>VREG1B/V</th></tr>
<tr><td>7'h00</td><td>4.8</td><td>0.3</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>N</td><td>(N+40)*0.02+4</td><td>N*0.02+0.3</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>7’h55</td><td>6.5</td><td>2.0</td></tr>
<tr><td>7’h56</td><td>reserved</td><td>reserved</td></tr>
<tr><td>…</td><td>…</td><td></td></tr>
<tr><td>7’h7F</td><td>reserved</td><td>reserved</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>vreg1_vbp_d[6:0]</th></tr>
<tr><td>Power On Sequence</td><td>7h3c</td></tr>
<tr><td>SW Reset</td><td>7h3c</td></tr>
<tr><td>HW Reset</td><td>7h3c</td></tr>
</table></td></tr>
</table>

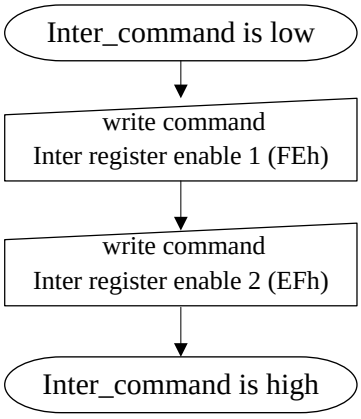
5.5.5.Power Control 3 (C4h)

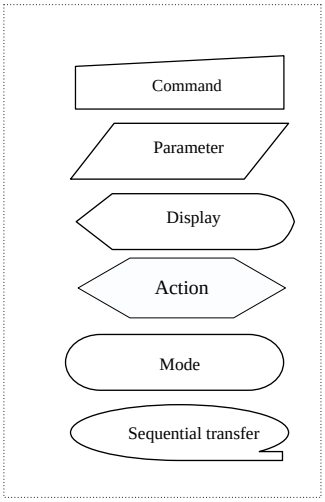
<table>
<tr><td>C4h</td><td colspan="13">Power Control 3</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>C4h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="7">vreg1_vbn_d[6:0]</td><td>3C</td></tr>
<tr><td>Description</td><td colspan="13">Set the voltage level value to output the VREG2A OUT level, which is a reference level for the grayscale voltage level(Table is valid when vrh=0x28)
VREG2A=(vbn_d-vrh)*0.02-3.4
VREG2B=vbn_d*0.02+0.3
<table>
<tr><th>vreg1_vbn_d[6:0]</th><th>VREG2A/V</th><th>VREG2B/V</th></tr>
<tr><td>7'h00</td><td>-4.2</td><td>0.3</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>N</td><td>N*0.02-4.2</td><td>N*0.02+0.3</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>7’h55</td><td>-2.5</td><td>2.0</td></tr>
<tr><td>7’h56</td><td>reserved</td><td>reserved</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>7’h7F</td><td>reserved</td><td>reserved</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>vreg1_vbn_d[6:0]</th></tr>
<tr><td>Power On Sequence</td><td>7’h3C</td></tr>
<tr><td>SW Reset</td><td>7’h3C</td></tr>
<tr><td>HW Reset</td><td>7’h3C</td></tr>
</table></td></tr>
</table>

5.5.6.Power Control 4 (C9h)

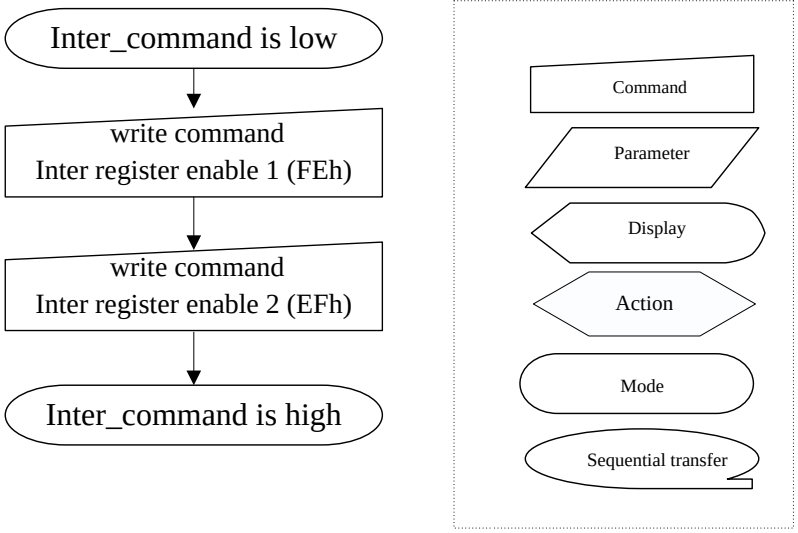
<table>
<tr><td>C9h</td><td colspan="13">Power Control 4</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>C9h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td colspan="6">vrh[5:0]</td><td>28</td></tr>
<tr><td>Description</td><td colspan="13">Set the voltage level value to output the VREG1A OUT level, which is a reference level for the grayscale voltage level. (Table is valid when vbp_d=0x3C and vbn_d=0x3C)
VREG1A=(vrh+vbp_d)*0.02+4
VREG2A=(vbn_d-vrh)*0.02-3.4
<table>
<tr><th>vrh[5:0]</th><th>VREG1A/V</th><th>VREG2A/V</th></tr>
<tr><td>6'h00</td><td>5.2</td><td>-2.2</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>N</td><td>(N+60)*0.02+4</td><td>(100-N)*0.02-4.2</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>6’h28</td><td>6</td><td>-3</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>6’h3F</td><td>6.46</td><td>-3.46</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>vrh[5:0]</th></tr>
<tr><td>Power On Sequence</td><td>6’h28</td></tr>
<tr><td>SW Reset</td><td>6’h28</td></tr>
<tr><td>HW Reset</td><td>6’h28</td></tr>
</table></td></tr>
</table>

5.5.7.Inter Register Enable1(FEh)

<table>
<tr><td>FEh</td><td colspan="12">Inter register enable 1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>FEh</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command is used for Inter_command controlling.
To set Inter_command high ,you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously.
Once Inter_command is set high, only hardware or software reset can turn it to low.
 


</td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="12"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12"></td></tr>
</table>

5.5.8.Inter Register Enable2(EFh)

<table>
<tr><td>EFh</td><td colspan="13">Inter register enable 2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>EFh</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used for Inter_command controlling.
To set Inter_command high ,you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously.
Once Inter_command is set high, only hardware or software reset can turn it to low.
 
</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13"></td></tr>
</table>

5.5.9.SET_GAMMA1 (F0h)

<table>
<tr><td>F0h</td><td colspan="13">SET_GAMMA1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>F0h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="2">dig2gam_dig2j0_n[1:0]</td><td colspan="6">dig2gam_vr1_n[5:0]</td><td>80</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="2">dig2gam_dig2j1_n[1:0]</td><td colspan="6">dig2gam_vr2_n[5:0]</td><td>03</td></tr>
<tr><td>3st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="3"></td><td colspan="5">dig2gam_vr4_n[4:0]</td><td>08</td></tr>
<tr><td>4nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="3"></td><td colspan="5">dig2gam_vr6_n[4:0]</td><td>06</td></tr>
<tr><td>5st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="5">dig2gam_vr0_n[3:0]</td><td colspan="3">dig2gam_vr13_n[3:0]</td><td>05</td></tr>
<tr><td>6nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="2"></td><td colspan="6">dig2gam_vr20_n[6:0]</td><td>2B</td></tr>
<tr><td>Description</td><td colspan="13">dig2gam_dig2j0_n[1:0]: γ gradient adjustment register for negative polarity
dig2gam_dig2j1_n[1:0]: γ gradient adjustment register for negative polarity
dig2gam_vr0_n[3:0]: γ gradient adjustment register for negative polarity
dig2gam_vr1_n[5:0]: γ gradient adjustment register for negative polarity
dig2gam_vr2_n[5:0]: γ gradient adjustment register for negative polarity
dig2gam_vr4_n[4:0]: γ gradient adjustment register for negative polarity
dig2gam_vr6_n[4:0]: γ gradient adjustment register for negative polarity
dig2gam_vr13_n[3:0]: γ gradient adjustment register for negative polarity
dig2gam_vr20_n[6:0]: γ gradient adjustment register for negative polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Ide Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

Default		Status	Default Value				
			dig2gam_dig2j0_n[1:0]	dig2gam_dig2j1_n[1:0]	dig2gam_vr0_n[3:0]	dig2gam_vr1_n[5:0]	dig2gam_vr2_n[5:0]	dig2gam_vr4_n[4:0]
		Power On Sequence	2'h02	2'h00	4'h00	6'h00	6'h03	5'h08
		SW Reset	2'h02	2'h00	4'h00	6'h00	6'h03	5'h08
		HW Reset	2'h02	2'h00	4'h00	6'h00	6'h03	5'h08

Default		Status	Default Value				
			dig2gam_vr6_n[4:0]	dig2gam_vr13_n[3:0]	dig2gam_vr20_n[6:0]			
		Power On Sequence	5'h06	4'h05	7'h2b			
		SW Reset	5'h06	4'h05	7'h2b			
		HW Reset	5'h06	4'h05	7'h2b			

5.5.10. SET_GAMMA2 (F1h)

<table>
<tr><td>F1h</td><td colspan="13">SET_GAMMA2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>F1h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td colspan="7">dig2gam_vr43_n[6:0]</td><td>41</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="3">dig2gam_vr27_n[2:0]</td><td colspan="5">dig2gam_vr57_n[4:0]</td><td>97</td></tr>
<tr><td>3st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="3">dig2gam_vr36_n[2:0]</td><td colspan="5">dig2gam_vr59_n[4:0]</td><td>98</td></tr>
<tr><td>4nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td colspan="6">dig2gam_vr61_n[5:0]</td><td>13</td></tr>
<tr><td>5st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td colspan="6">dig2gam_vr62_n[5:0]</td><td>17</td></tr>
<tr><td>6nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="4">dig2gam_vr50_n[3:0]</td><td colspan="4">dig2gam_vr63_n[3:0]</td><td>CD</td></tr>
<tr><td>Description</td><td colspan="13">dig2gam_vr43_p[6:0]: γ gradient adjustment register for negative polarity
dig2gam_vr27_p[2:0]: γ gradient adjustment register for negative polarity
dig2gam_vr57_p[4:0]: γ gradient adjustment register for negative polarity
dig2gam_vr59_p[4:0]: γ gradient adjustment register for negative polarity
dig2gam_vr36_p[2:0]: γ gradient adjustment register for negative polarity
dig2gam_vr61_p[5:0]: γ gradient adjustment register for negative polarity
dig2gam_vr62_p[5:0]: γ gradient adjustment register for negative polarity
dig2gam_vr50_p[3:0]: γ gradient adjustment register for negative polarity
dig2gam_vr63_p[3:0]: γ gradient adjustment register for negative polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Moe On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

Default

Status	Default Value					
	dig2gam_vr43_p[6:0]	dig2gam_vr27_p[2:0]	dig2gam_vr57_p[4:0]	dig2gam_vr59_p[4:0]	dig2gam_vr36_p[2:0]	dig2gam_vr61_p[5:0]
Power On Sequence	7'h41	3'h04	5'h17	5'h18	3'h04	6'h13
SW Reset	7'h41	3'h04	5'h17	5'h18	3'h04	6'h13
HW Reset	7'h41	3'h04	5'h17	5'h18	3'h04	6'h13

Default

Status	Default Value					
	dig2gam_vr62_p[5:0]	dig2gam_vr50_p[3:0]	dig2gam_vr63_p[3:0]			
Power On Sequence	6'h17	4'h0C	4'h0D			
SW Reset	6'h17	4'h0C	4'h0D			
HW Reset	6'h17	4'h0C	4'h0D			

5.5.11. SET_GAMMA3 (F2h)

<table>
<tr><td>F2h</td><td colspan="13">SET_GAMMA3</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>F2h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="2">dig2gam_dig2j0_p[1:0]</td><td colspan="6">dig2gam_vr1_p[5:0]</td><td>40</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="2">dig2gam_dig2j1_p[1:0]</td><td colspan="6">dig2gam_vr2_p[5:0]</td><td>03</td></tr>
<tr><td>3st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td></td><td colspan="5">dig2gam_vr4_p[4:0]</td><td>08</td></tr>
<tr><td>4nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td></td><td colspan="5">dig2gam_vr6_p[4:0]</td><td>0B</td></tr>
<tr><td>5st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="4">dig2gam_vr0_p[3:0]</td><td colspan="4">dig2gam_vr13_p[3:0]</td><td>08</td></tr>
<tr><td>6nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td colspan="7">dig2gam_vr20_p[6:0]</td><td>2E</td></tr>
<tr><td>Description</td><td colspan="13">dig2gam_dig2j0_p[1:0]: γ gradient adjustment register for positive polarity
dig2gam_dig2j1_p[1:0]: γ gradient adjustment register for positive polarity
dig2gam_vr1_p[5:0]: γ gradient adjustment register for positive polarity
dig2gam_vr2_p[5:0]: γ gradient adjustment register for positive polarity
dig2gam_vr4_p[4:0]: γ gradient adjustment register for positive polarity
dig2gam_vr6_p[4:0]: γ gradient adjustment register for positive polarity
dig2gam_vr0_p[3:0]: γ gradient adjustment register for positive polarity
dig2gam_vr13_p[3:0]: γ gradient adjustment register for positive polarity
dig2gam_vr20_p[6:0]: γ gradient adjustment register for positive polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mde Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

Default

Status	Default Value					
	dig2gam_dig2j0_p[1:0]	dig2gam_dig2j1_p[1:0]	dig2gam_vr1_p[5:0]	dig2gam_vr2_p[5:0]	dig2gam_vr4_p[4:0]	dig2gam_vr6_p[4:0]
Power On Sequence	2'h01	2'h00	6'h00	6'h03	5'h08	5'h0B
SW Reset	2'h01	2'h00	6'h00	6'h03	5'h08	5'h0B
HW Reset	2'h01	2'h00	6'h00	6'h03	5'h08	5'h0B

Default

Status	Default Value					
	dig2gam_vr0_p[3:0]	dig2gam_vr13_p[3:0]	dig2gam_vr20_p[6:0]			
Power On Sequence	4'h00	4'h08	7'h2E			
SW Reset	4'h00	4'h08	7'h2E			
HW Reset	4'h00	4'h08	7'h2E			

5.5.12. SET_GAMMA4 (F3h)

<table>
<tr><td>F3h</td><td colspan="13">SET_GAMMA4</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>F3h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td colspan="7">dig2gam_vr43_p[6:0]</td><td>3F</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="2">dig2gam_vr27_p[2:0]</td><td colspan="6">dig2gam_vr57_p[4:0]</td><td>98</td></tr>
<tr><td>3st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="2">dig2gam_vr36_p[2:0]</td><td colspan="6">dig2gam_vr59_p[4:0]</td><td>B4</td></tr>
<tr><td>4nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td colspan="6">dig2gam_vr61_p[5:0]</td><td>14</td></tr>
<tr><td>5st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td colspan="6">dig2gam_vr62_p[5:0]</td><td>18</td></tr>
<tr><td>6nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="4">dig2gam_vr50_p[3:0]</td><td colspan="4">dig2gam_vr63_p[3:0]</td><td>CD</td></tr>
<tr><td>Description</td><td colspan="13">dig2gam_vr43_p[6:0]: γ gradient adjustment register for positive polarity
dig2gam_vr27_p[2:0]: γ gradient adjustment register for positive polarity
dig2gam_vr57_p[4:0]: γ gradient adjustment register for positive polarity
dig2gam_vr36_p[2:0]: γ gradient adjustment register for positive polarity
dig2gam_vr59_p[4:0]: γ gradient adjustment register for positive polarity
dig2gam_vr61_p[5:0]: γ gradient adjustment register for positive polarity
dig2gam_vr62_p[5:0]: γ gradient adjustment register for positive polarity
dig2gam_vr50_p[3:0]: γ gradient adjustment register for positive polarity
dig2gam_vr63_p[3:0]: γ gradient adjustment register for positive polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availbility</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

Default

Status	Default Value					
	dig2gam_vr43_p[6:0]	dig2gam_vr27_p[2:0]	dig2gam_vr57_p[4:0]	dig2gam_vr36_p[2:0]	dig2gam_vr59_p[4:0]	dig2gam_vr61_p[5:0]
Power On Sequence	7'h3F	3'h04	5'h18	3'h05	5'h14	6'h14
SW Reset	7'h3F	3'h04	5'h18	3'h05	5'h14	6'h14
HW Reset	7'h3F	3'h04	5'h18	3'h05	5'h14	6'h14

Default

Status	Default Value					
	dig2gam_vr62_p[5:0]	dig2gam_vr50_p[3:0]	dig2gam_vr63_p[3:0]			
Power On Sequence	6'h18	4'h0C	4'h0D			
SW Reset	6'h18	4'h0C	4'h0D			
HW Reset	6'h18	4'h0C	4'h0D			

6. Electrical Characteristics

6.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When GC9B71 is used out of the absolute maximum ratings, GC9B71 may be permanently damaged. To use GC9B71 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, GC9B71 will malfunction and cause poor reliability.

Table43.

Item	Symbol	Unit	Value
Supply voltage	VDDB	V	-0.3~+4.6
Supply voltage(Logic)	VDDI	V	-0.3~+4.6
Supply voltage(Digital)	DVDD	V	-0.3~+2.0
Driver supply voltage	VGH-VGL	V	-0.3~+27.0
Logic input voltage range	VIN	V	-0.3~VDDI+0.3
Logic output voltage range	VO	V	-0.3~VDDI+0.3
Operation temperature	Topr	℃	-40~+80
Storage temperature	Tstg	℃	-40~+80
Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.			

6.2. DC Characteristics

6.2.1. DC Characteristics for Panel Driving

General DC Characteristics

Table44.

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VDDB	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	VDDI	V	I/O supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	DVDD	V	Digital supply voltage	-	1.5	-	Note2
Gate Driver High Voltage	VGH	V	-	8.0	-	15.0	Note3
Gate Driver Low Voltage	VGL	V	-	-12.0	-	-7.0	Note3
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7*VDDI	-	VDDI	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	VSSB	-	0.3*VDDI	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*VDDI	-	VDDI	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	VSSB	-	0.2*VDDI	Note1,2,3
Logic High Level Input Current	IIH	uA	-	-	-	1	Note1,2,3
Logic Low Level Input Current	IIL	uA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=VDDI or VSSB	-0.1	-	+0.1	Note1,2,3
Source Driver							
Positive Source Output Range	Vsout	V	-	VREG1B	-	VREG1A	
Negative Source Output Range	Vsout	V	-	VREG2A	-	VREG2B	

Note 1: VDDI=1.65 to 3.3V, VDDB=2.5 to 3.3V, AGND=VSS=0V, Ta=-30 to 70 (to +85 no damage)℃

Note2: Please supply digital VDDI voltage equal or less than analog VDDB voltage.

Note3: CSX, RDX, WRX, D[7:0], D/CX, RESX, TE, SDA, SCL, IM2, IM1,IM0, and Test pins.

6.2.2. DC characteristics for DSI LP mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined on table below: DC Characteristics for DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned on the condition column. Other logical levels of the table are for MCU interface.

parameter	symbol	condition	Specification			Unit
			Min.	Typ.	Max.	
Logic High level output voltage	V_{OH}	I_{OUT}=-1mA ;Note 2	0.8IOVCC	-	IOVCC	V
Logic Low level output voltage	V_{OL}	I_{OUT}=-1mA ; Note 2	0.0	-	0.2 IOVCC	V
Logic High level input voltage	V_{IHLPCD}	LP-CD ; Note 3	450	-	1350	mV
Logic Low level input voltage	V_{ILLPCD}	LP-CD ; Note 3	0.0	-	200	mV
Logic High level input voltage	V_{IHLPRX}	LP-RX (CLOCK, DATA) ; Note 3	880	-	1350	mV
Logic Low level input voltage	V_{ILLPRX}	LP-RX (CLOCK, DATA) ; Note 3	0.0	-	550	mV
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLOCK ULP mode), Note 3	0.0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (DATA), Note 3	1.1	-	1.3	V
Logic Low level output voltage	V_{OLLPTX}	LP-TX (DATA), Note 3	-50	-	50	mV
Logic High level input current	I_{IH}	LP-CD, LP-RX, Note 3	-	-	10	uA
Logic Low level input current	I_{IL}	LP-CD, LP-RX, Note 3	-10	-	-	uA

Note: (1) Ta=-30℃ to 70℃ (to +85℃ no damage)

(2) PWM_OUT, TE

(3) DSI High Speed mode is off

6.2.3. DC characteristics for DSI HS mode

DC levels of the HS-0 and HS-0 are defined on table below: DC Characteristics for DSI HS mode.

parameter	symbol	condition	Specification			Unit
			Min.	Typ.	Max.	
Input Common Mode Voltage for Clock	V_{CMCLK}	DSI-CLOCK_P/N ; Note 2,3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DSI-DATA_P/N ; Note 2,3	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	DSI-CLOCK_P/N ; Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DSI-DATA_P/N ; Note 4	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	DSI-CLOCK_P/N	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DSI-DATA_P/N	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	DSI-CLOCK_P/N	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DSI-DATA_P/N	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	DSI-CLOCK_P/N	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DSI-DATA_P/N	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	DSI-CLOCK_P/N, DSI-DATA_P/N ; Note 3	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	DSI-CLOCK_P/N, DSI-DATA_P/N ; Note 3	-	-	460	mV
Differential Termination Resistor	R_{TERM}	DSI-CLOCK_P/N, DSI-DATA_P/N	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	DSI-CLOCK_P/N, DSI-DATA_P/N	-	-	450	mV

Termination Capacitor	C_{TERM}	DSI-CLOCK_P/N, DSI-DATA_P/N	-	-	14	pF

Note: (1) Ta = -30 to 70 °C (to +85 °C no damage), IOVCC = 1.65 to 1.95V, GND = 0V

(2) Includes 50mV (-50mV to 50mV) ground difference

(3) Without $V_{CMRCLKM450}$/$V_{CMRDATAM450}$

(4) Without 50mV (-50mV to 50mV) ground difference

6.3. AC Characteristics

6.3.1. Display Parallel 8-bit Interface Timing Characteristics (8080-I)

Figure90.

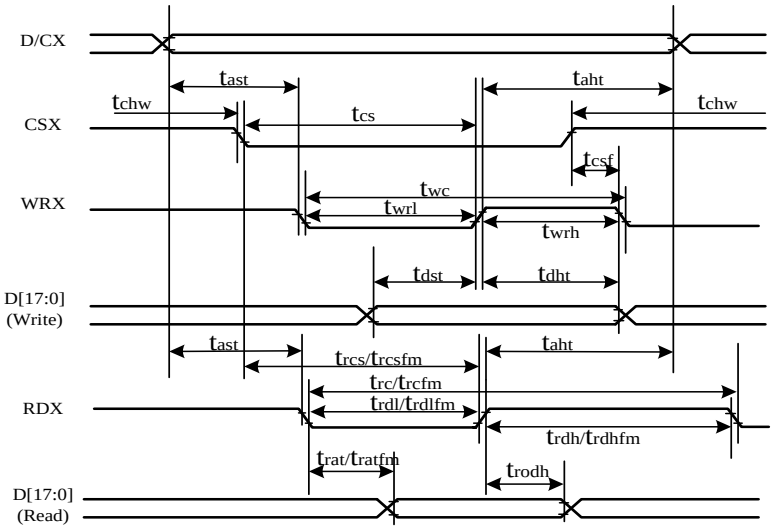
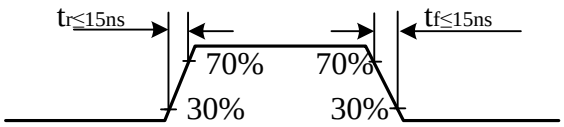


Table45.

Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	380	-	ns	
	trdhfm	Read Control H duration(FM)	180	-	ns	
	trdlfm	Read Control L duration(FM)	200	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control H pulse duration	90	-	ns	
	trdl	Read Control L pulse duration	70	-	ns	
D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

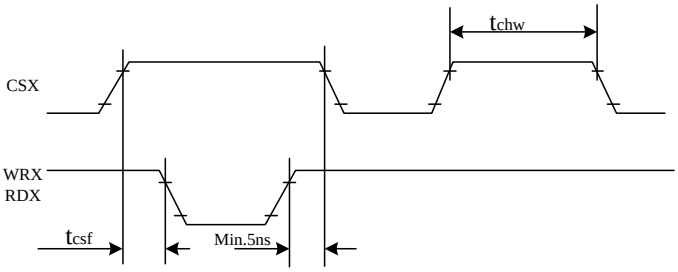
Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDDB=2.5V to 3.3V, VSS=0V

Figure91.



CSX timings :

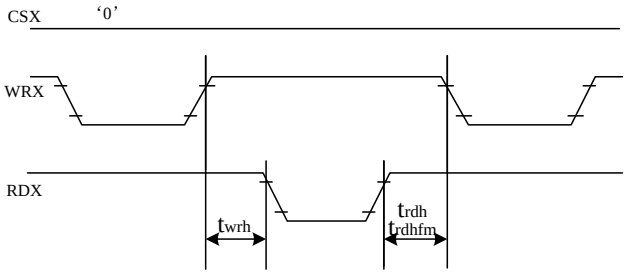
Figure92.



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:

Figure92.



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

6.3.2. Display Serial Interface Timing Characteristics (3-line SPI system)

Figure97.

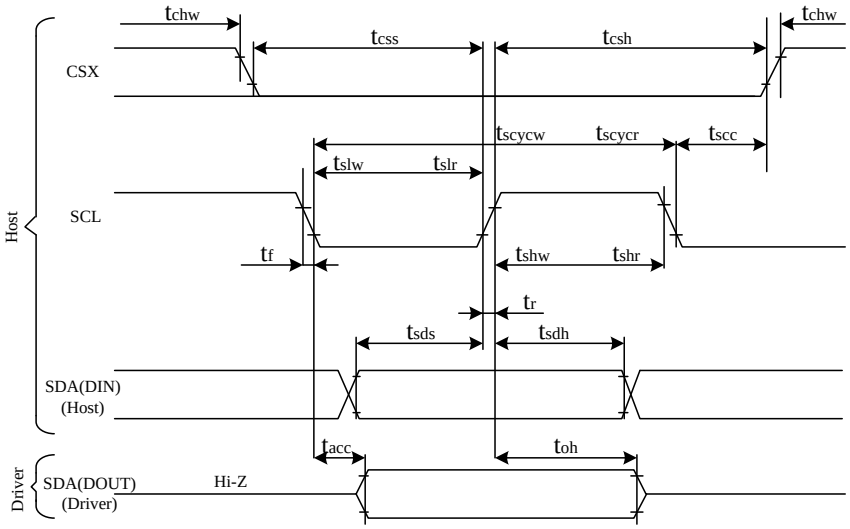
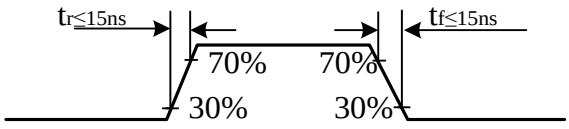


Table47.

Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	10	-	ns	
	tshw	SCL "H" Pulse Width (Write)	5	-	ns	
	tslw	SCL "L" Pulse Width (Write)	5	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA /D0 (Input)	tsds	Data setup time (Write)	5	-	ns	
	tsdh	Data hold time (Write)	5	-	ns	
SDA/D0 (Output)	tacc	Access time (Read)	10	-	ns	
CSX	tscc	SCL-CSX	10	-	ns	
	tchw	CSX "H" Pulse Width	10	-	ns	
	tcss	CSX-SCL Time	20	-	ns	
	tcsh		40	-	ns	

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VDDB=2.5V to 3.3V, VSSB=VSSB=0V

Figure98.



6.3.3. Display Serial Interface Timing Characteristics (4-line SPI system)

Figure98.

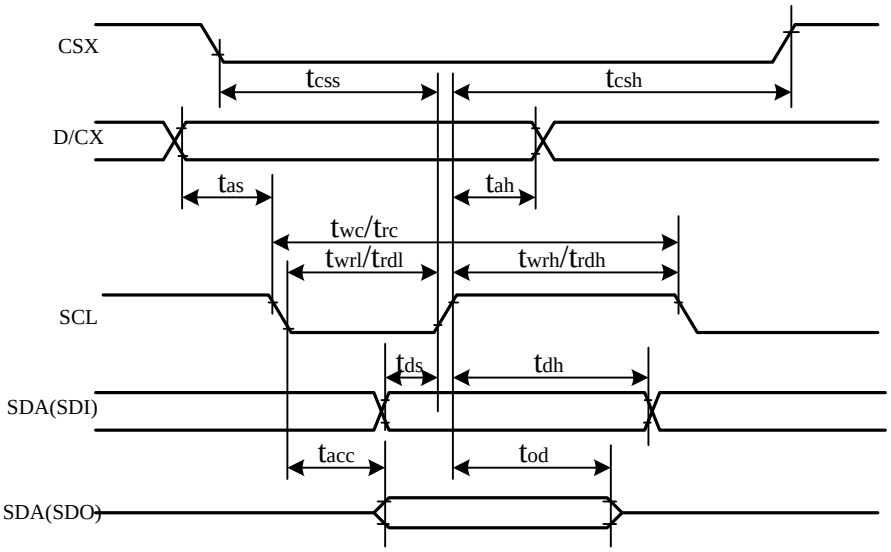
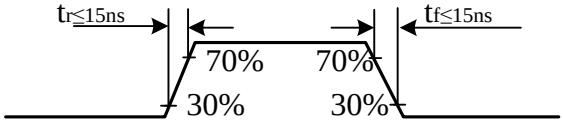


Table48.

Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	20	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial Clock Cycle (Write)	10	-	ns	
	twrh	SCL "H" Pulse Width (Write)	5	-	ns	
	twrl	SCL "L" Pulse Width (Write)	5	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL "H" Pulse Width (Read)	60	-	ns	
	trdl	SCL "L" Pulse Width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA/D0 (Input)	tds	Data setup time (Write)	5	-	ns	
	tdh	Data hold time (Write)	5	-	ns	
SDA/D0 (Output)	tacc	Access time (Read)	10	-	ns	

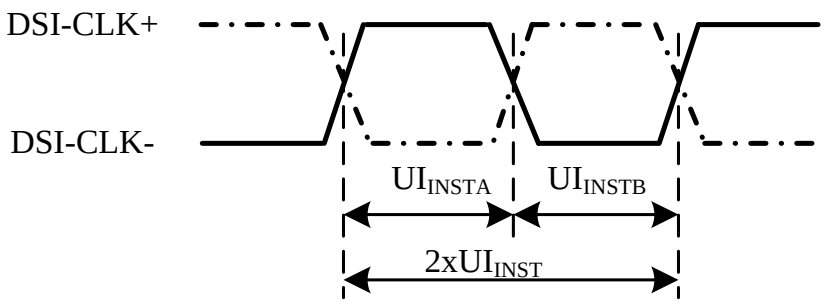
Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VDDB=2.5V to 3.3V, AGND=VSS=0V

Figure99.



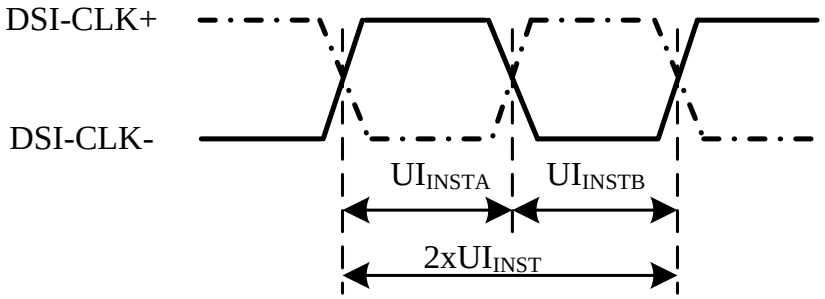
6.4. MIPI

6.4.1. High Speed Mode – Clock Channel Timing

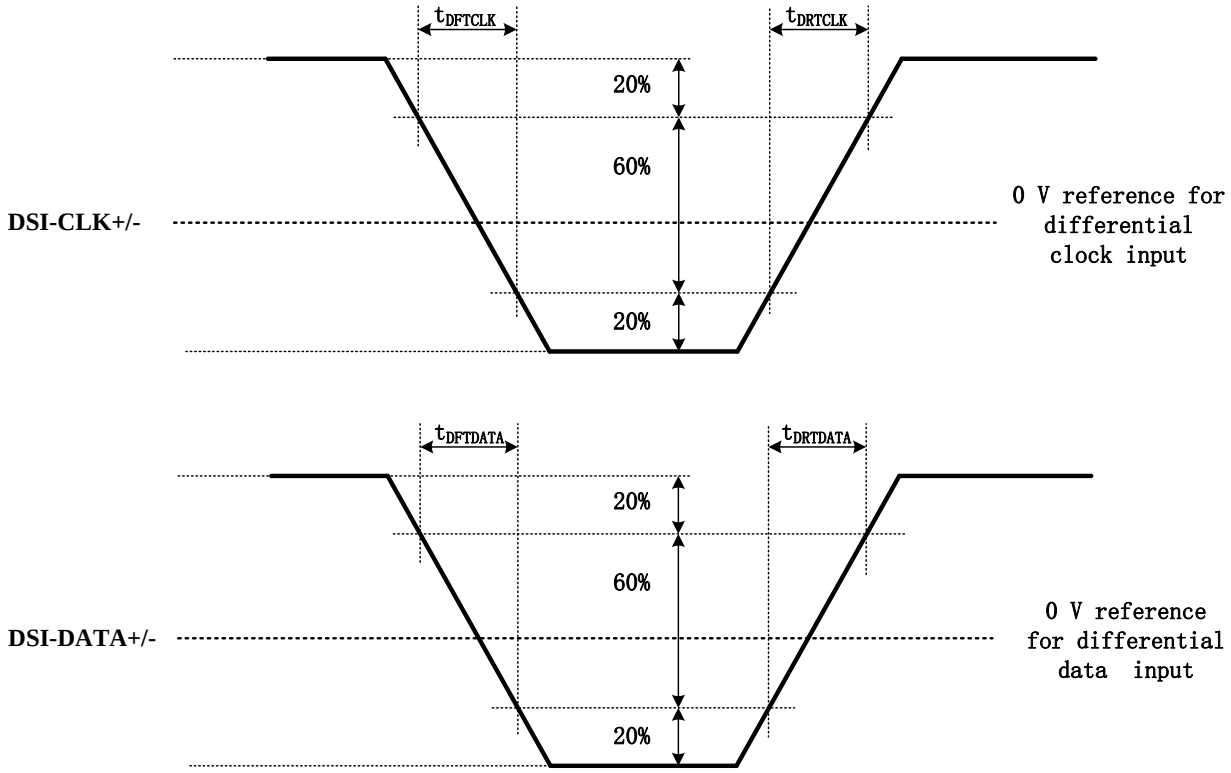


Signal	Symbol	Parameter	Min	Max	Unit
DSI_CLOCK_P/N	$2xUI_{INST}$	Double UI instantaneous	8	25	ns
DSI_CLOCK_P/N	UI_{INSTA}, UI_{INSTB}	UI instantaneous Half	4	12.5	ns

Note: UI = UI_{INSTA} = UI_{INSTB}

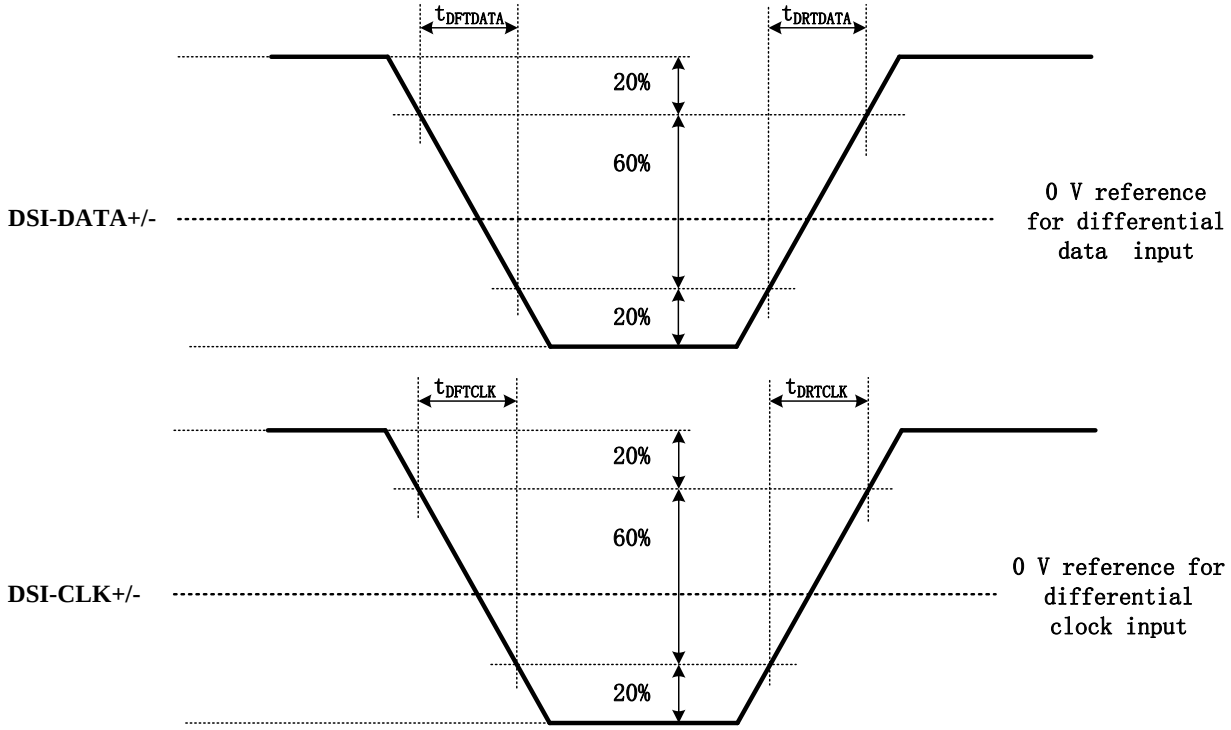


6.4.2. High Speed Mode – Rise and Fall Timings



Signal	Symbol	Condition	specification			Unit
			Min	Max	Type	
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLOCK_P/N	-	-	900	ps
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-DATA_P/N	-	-	900	ps
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLOCK_P/N	-	-	900	Ps
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-DATA_P/N	-	-	900	ps

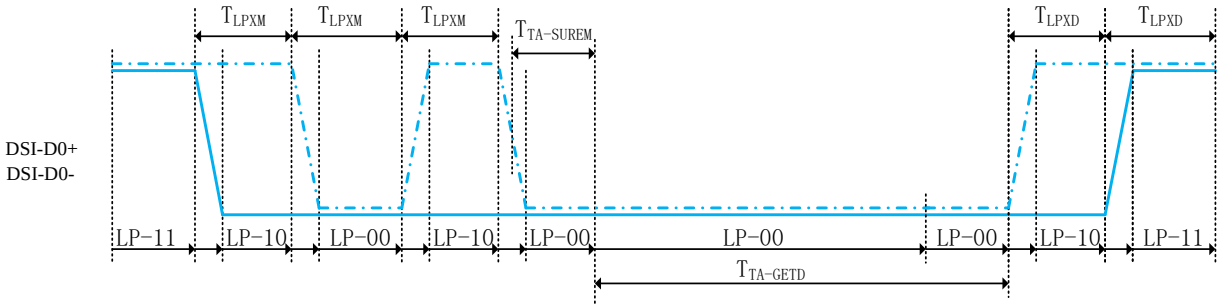
6.4.3. High Speed Mode – Rise and Fall Timings



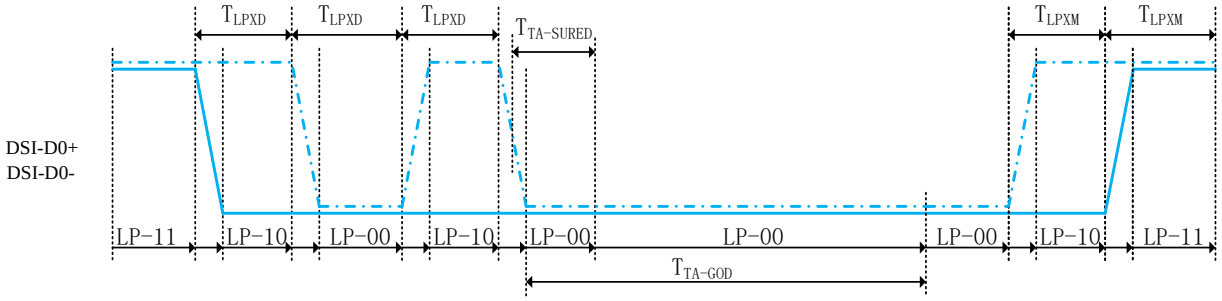
Signal	Symbol	Condition	specification			Unit
			Min	Max	Type	
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLOCK_P/N	-	-	900	ps
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-DATA_P/N	-	-	900	ps
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLOCK_P/N	-	-	900	Ps
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-DATA_P/N	-	-	900	ps

6.4.4. Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MCU to the GC9B71sequence below.



Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from GC9B71to the MCU sequence below.

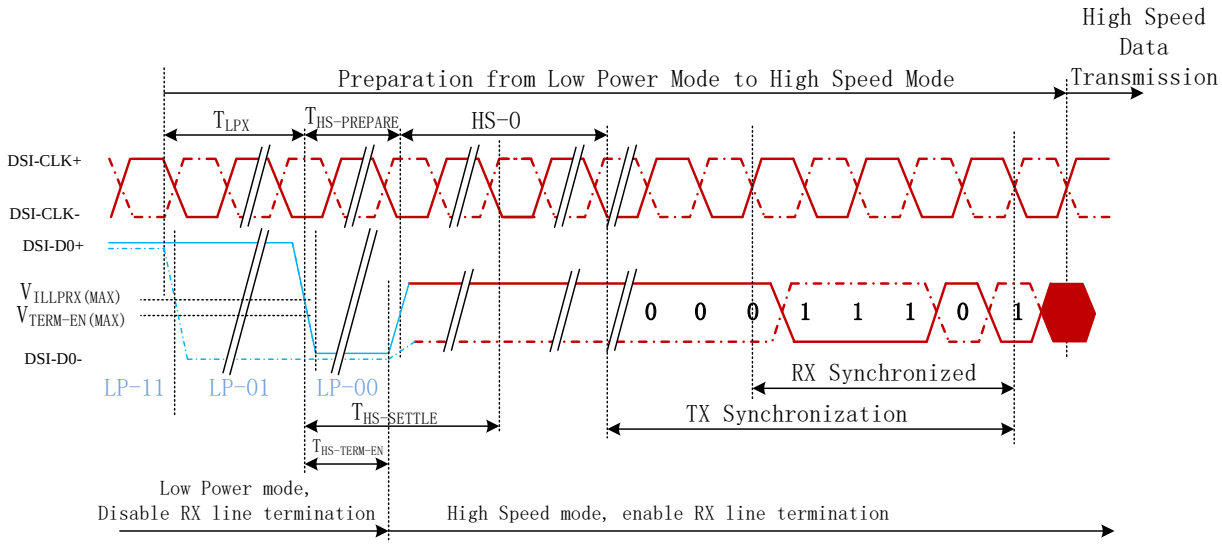


Signal	Symbol	Description	Min	Max	Unit
Input (DSI-DATA_P/N)	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → GC9B71	50	-	ns
Input (DSI-DATA_P/N)	$T_{TA-SUREM}$	Time-out before the GC9B71starts driving	T_{LPXM}	$2xT_{LPXM}$	ns
Output (DSI-DATA_P/N)	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods GC9B71→ MCU	50	75	ns
Output (DSI-DATA_P/N)	$T_{TA-SURED}$	Time-out before the MCU starts driving	T_{LPXD}	$2xT_{LPXD}$	

7.

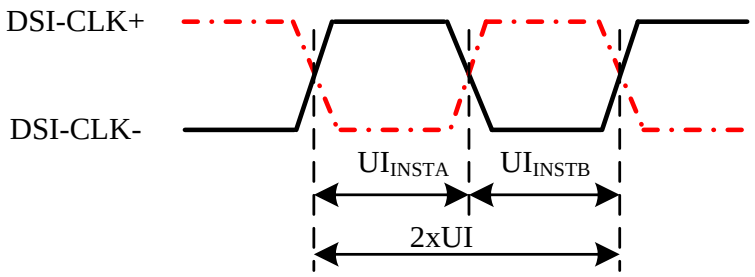
Signal	Symbol	Description	Time	Unit
Input (DSI-DATA_P/N)	$T_{TA-GETD}$	Time to drive LP-00 by GC9B71	$5xT_{LPXD}$	ns
Output (DSI-DATA_P/N)	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

6.4.5. Data Lanes from Low Power Mode to High Speed Mode

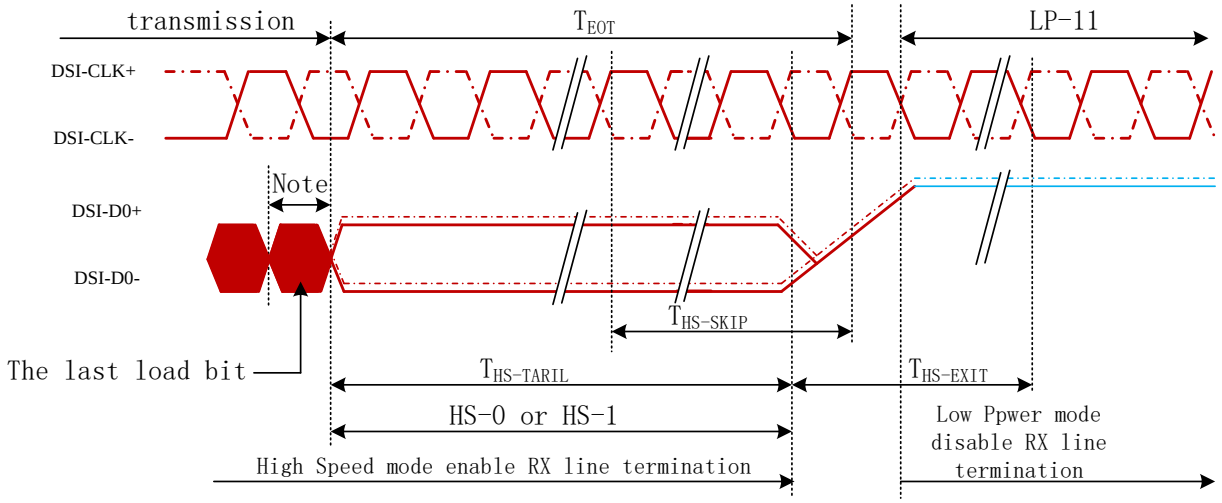


Signal	Symbol	Description	Min	Max	Unit
Input (DSI-DATA_P/N)	T_{LPX}	Length of any low power state period	50	-	ns
Input (DSI-DATA_P/N)	$T_{HS-PREPARE}$	Time to Drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
Input (DSI-DATA_P/N)	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses V_{ILMAX}	-	35+4xUI	ns

Note: UI definition: UI = UI_{INSTA} = UI_{INSTB}



6.4.6. Data Lanes from High Speed Mode to Low Power Mode



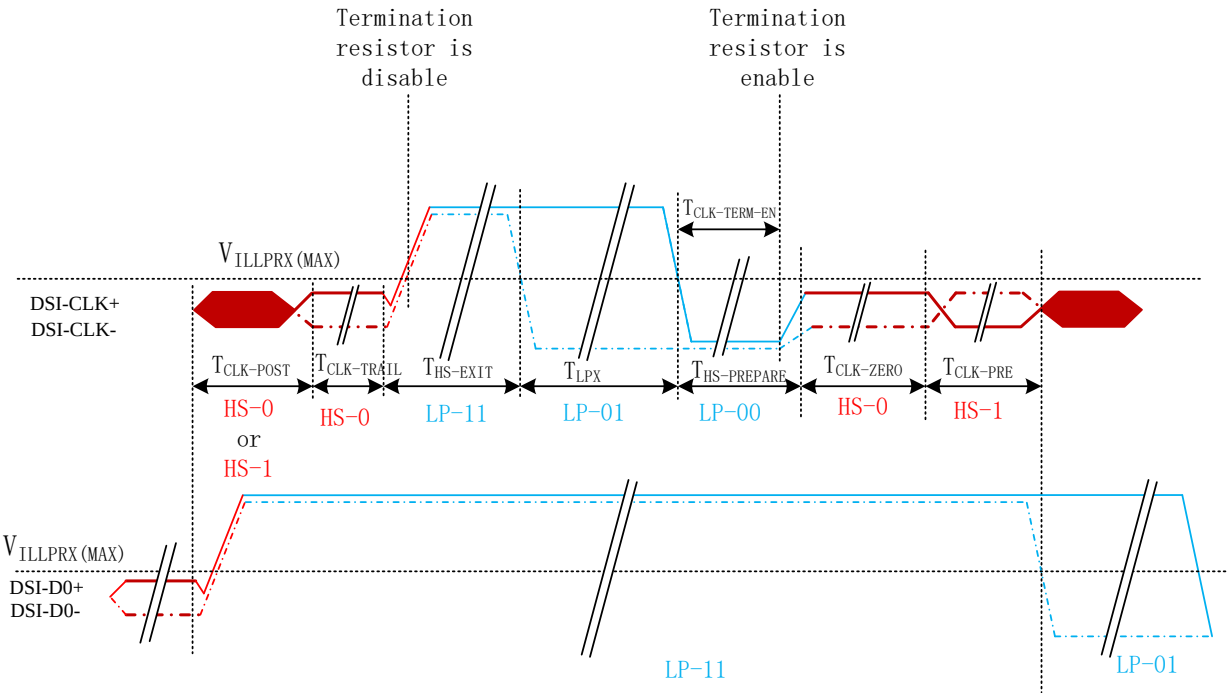
Note:

If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

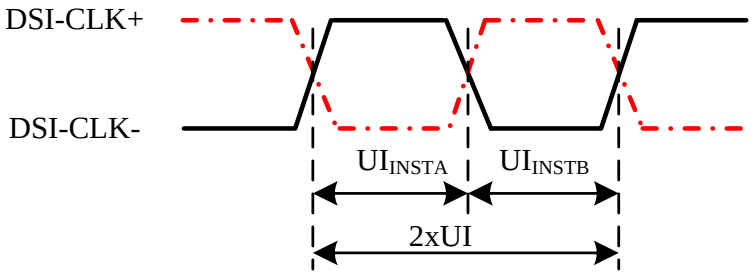
Signal	Symbol	Description	Min	Max	Unit
Input (DSI-DATA_P/N)	$T_{TA-SKIP}$	Time-out at GC9B71to Ignore Transition Period of EoT	40	4xUI	ns
Output (DSI-DATA_P/N)	$T_{TA-EXIT}$	Time to Driver LP-11 after HS burst	100	-	ns

6.4.7.DSI Clock Burst – High Speed Mode to/from Low Power Mode



Signal	Symbol	Description	Min	Max	Unit
Input (DSI-DATA_P/N)	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
Input (DSI-DATA_P/N)	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
Input (DSI-DATA_P/N)	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
Input (DSI-DATA_P/N)	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	
Input (DSI-DATA_P/N)	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	38	-	
Input (DSI-DATA_P/N)	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300		
Input (DSI-DATA_P/N)	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI		

Note: UI definition: $UI = UI_{INSTA} = UI_{INSTB}$


DSI-CLK+
DSI-CLK-
UI_INSTA
UI_INSTB
2xUI